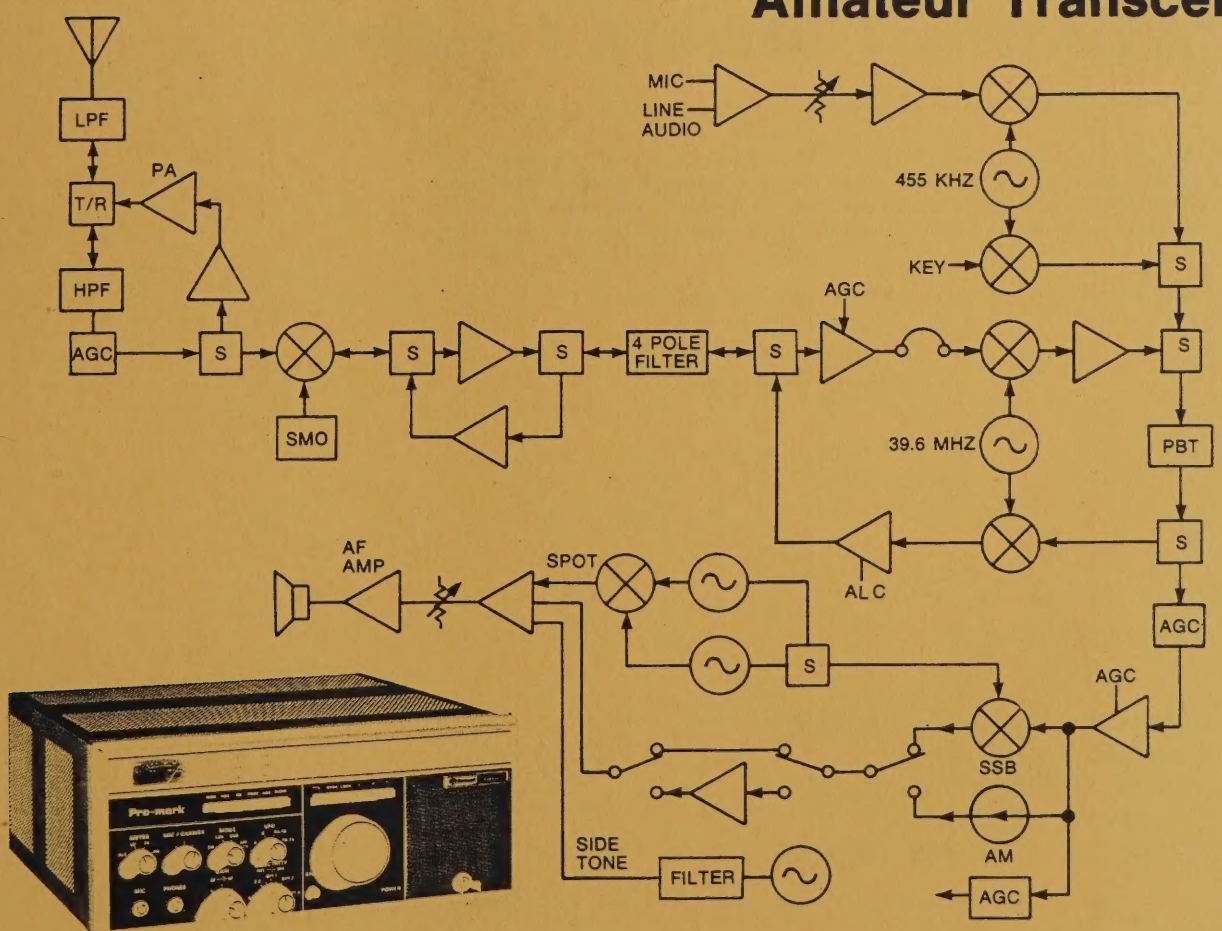
Rockwell International

training manual

Collins Telecommunications Products Division

Collins KWM-380 Amateur Transceiver



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Self-Study Training Course on the Collins KWM-380 Transceiver

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The KWM-380 training manual has been prepared by the Customer Training Department, Collins Telecommunication Products Division of Rockwell International, Cedar Rapids, Iowa. The information contained in this manual parallels and supplements the information contained in the Owner's Manual and Service Manual for the KWM-380. This material is, however, prepared for the express purpose of training. When used with the tape-cassettes and Service Manual it becomes part of an individualized training course, when used separately, it is a ready reference for the KWM-380 operation.

To begin the program, insert tape number one side 1 into a tape recorder and follow the oral instructions.

The course consists of several cassette tapes and the self-study training manual. The following guidelines should be followed.

a. Follow the speaker when referring to figure, page number, or tables.

b. Do not try to read the written material in the manual and listen to the tape at the same time. Listen to a portion of the tape, turn off the recorder and review the material just covered on the tape by reading the corresponding section of the manual.

c. Complete the exercises at the end of each topic before continuing.

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1.1 INTRODUCTION

1.1.1 Objectives

The students' objectives for section 1 of this training manual are as follows:

a. Learn the major components (assemblies of the transceiver).
b. Know the important parameters (specifications) of the system.
c. Learn the description of each major assembly.
d. Understand the installation and operation of the KWM-380.

1.1.2 General

The KWM-380 is a microprocessor controlled, fully synthesized, all solid-state transceiver. Full coverage from 29.99999 down to 0.50000 MHz is standard in the receiver circuits. Transmission is limited to 1.800 to 2.000, 3.500 to 4.000, 7.000 to 7.300, 14.000 to 14.350, 21.000 to 21.450 and 28.000 to 29.700 MHz in the amateur radio service bands.

Rate-selectable tuning permits rapid frequency changing without a band switch. The operator can change frequency in megahertz increments by pressing the button below the megahertz display. By pressing other buttons in the same row, frequency changes in kilohertz, hundred hertz and ten hertz can be made.

Microprocessor technology used in the KWM-380 provides an innovative but simple way for split-frequency operation of the radio. Storage registers A and B are loaded - one with the transmit frequency and other with the receive frequency. The vfo selector is then used to determine which register will transmit and which will receive. Pushing the SYNC button will cause the frequency of the register in use to also appear in the other register for simplex operation. The microprocessor is also used to make remote control possible by providing ten optional programmable frequency registers. These are accessible at the rear connector using an external key pad with the optional control interface kit. Frequency spotting with the KWM-380 is accomplished by audibly comparing the frequency of the receive signal with the frequency generated by pressing the spot button. Adjusting the receive frequency to match the audible tone sets the transmit frequency squarely on the receive frequency.

If passband selectivity is determined by turning the selectivity knob on the front panel. When severe interference occurs, the passband can be moved up or down frequency to escape the interfering signal. The KWM-380 is factory equipped with 8.0 and 2.2 kilohertz bandpass filters. Three optional positions are available for other services, such as radio teletype, or CW operation.

Special components in the KWM-380 give it a wide dynamic signal range of about 20 dB at the third-order intercept point, this reduces the intermod distortion from nearby stations, and lowers front end desensitizing from a strong AGC. An effective noise blanker is available in the KWM-380 to reduce the effects of inpulse noise.

In continuous duty operation, such as radio teletype hookups, the basic radio has a rated output of 50 watts. With the optional blower kit, the output is rated at one hundred watts. The use of broadband circuitry in the KWM-380 eliminates the need for tuning and peaking the exciter and final amplifier. A plug-in speech processing card is available as an option. With speech processing, the average talk power is significantly increased.

The built-in power supply of the KWM-380 allows operation of the unit from either a standard ac source of 115 or 230 volts, or a 12-volt dc source. Maintenance ease was emphasized throughout the design of the KWM-380. All circuit cards are easily accessible by removing the top and bottom covers, and the cards contain test points for parameter measurements.

Equipment modifications to accommodate potential amateur band changes can be readily accomplished in the future.

1.2 TECHNICAL CHARACTERISTICS OF THE KWM-380 TRANSCEIVER

1.2.1 Physical

Size	394 mm (15.5 in) wide, 165 mm (6.5 in) high, (does not include 25 mm (1 in) feet normally attached), 457 mm (18.0 in) deep.
Weight	21.8 kg (48 lbs) max.

1.2.2 Primary Power

Strappable for: 105, 115, 125/210, 220, 230, 240, 250 V ±5%, 50 to 60 Hz; or 12 to 15 V dc. 120 W max in receive; 600 W max in transmit.

1.2.3 Receiver

Frequency	0.5 to 30.0 MHz, tunable in 10-Hz steps.
Modes	USB, LSB, AM, and CW.
Sensitivity	0.5 μV or better for 10 dB (s+n)/n, 2.0 to 30.0 MHz; reduced sensitivity for 0.5 to 2.0 MHz (broadcast band attenuation nominally 30 dB).
Selectivity (3-dB bandwidth)	Selectable.

8 kHz	*1.7 kHz
*6 kHz	*400 Hz
2.1 kHz	*200 Hz

If and image rejection	Greater than 60 dB.
Intermodulation distortion	-50 dB or better for two signals of -10 dB mW each, 20 kHz apart.
AGC	Audio output variation not more than 8 dB for 2-μV to 100-mV open circuit rf input variation.

*optional filters

Audio output ..... Not less than 3.5 W into 4-ohm load, at 1 kHz, at no more than 10% total harmonic distortion.

< 10% distortion

Line audio output: -10 dB mW nominal into 600 ohms.

Frequency response: 300 to 2400 Hz with not more than 5 dB variation.

1.2.4 Transmitter

Frequency ..... 160- through 10-m amateur bands, tunable in 10-Hz steps.

160m	1.800 - 2.000 MHz
80/75m	3.500 - 4.000 MHz
40m	7.000 - 7.300 MHz
20m	14.000 - 14.350 MHz
15m	21.000 - 21.450 MHz
10m	28.000 - 29.700 MHz

Modes ..... USB, LSB, and CW.

Output power ..... 100 W pep, nominal.

In CW or RTTY, automatic turndown to 50 W after 10 seconds, 50 percent duty cycle, keydown 15 minutes, max.

With optional blower kit installed, power is 100 W average, 50 percent duty cycle, keydown 1 hour, max, at 25 °C; 30 minutes, max, at 50 °C for all modes.

1.2.5 Unwanted Signal Suppression

Carrier ..... -50 dB or better.

Undesired sideband, 1-kHz ref ..... -55 dB or better.

Harmonics (all) ..... -40 dB or better.

Mixer products ..... -55 dB or better.

Third order distortion ..... 25 dB below each tone of two-tone test.

1.2.6 Synthesizer accuracy and stability ..... Accuracy within ±5 Hz after 10 minutes warmup when 39.6- and 445-MHz oscillators are set to within ±3 Hz.

Stability within ±150 Hz over temperature range of 0 to 50 °C.

1.2.7 RF load ..... 50 ohms, nonreactive. Full power output with vswr of 2:1 or less. Automatic power output turndown with vswr greater than 2:1.

1.2.8 Audio inputs

Microphone	Low impedance, dynamic; internal strapping for high impedance. Units with serial numbers 51 and higher are factory wired for a nominal 3-kilohm microphone impedance. Either a low- or high-impedance dynamic microphone may be used without modification to the unit.
Line	600 ohm, unbalanced; 40-mV input sufficient for full rf power output.

1.3 FRONT PANEL CONTROLS AND INDICATORS

Figure 1-1 shows the front panel of the transceiver, refer to table 1-1 for a brief description of the front panel controls and indicators.

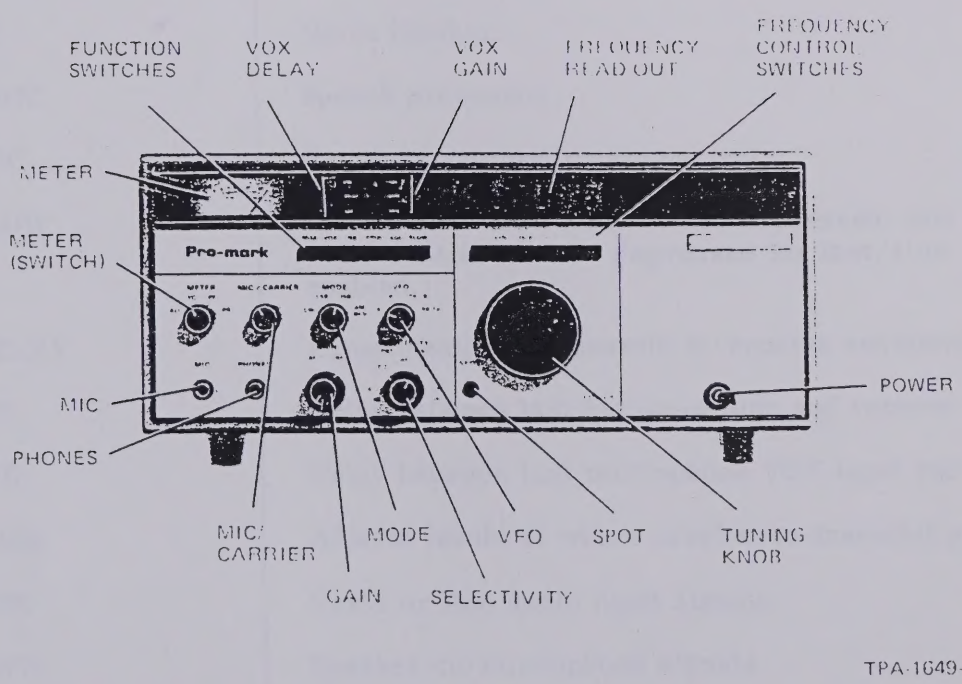


Figure 1-1. Front Panel Controls and Indicators.

Table 1-1. Front Panel Controls and Indicators.

ITEM	FUNCTION
METER (switch)	Selects signal applied to meter during transmit.
ALC	Transmitter automatic level control voltage.
VC	Collector voltage for final amplifier stage.
PF	Forward rf power sampled at amplifier output.
PR	Reflected rf power sampled at amplifier output.
Meter	In receive, indicates relative signal strength in :S: units. (Rf input of 100 V "hard" (50 V "soft") gives S9 indication.) In transmit, indicates signal selected by METER switch.
Function switches	Selects related function when switch depressed.
MOX	Manually operated receive-to-transmit switching. Places transceiver in transmit when pressed.
VOX	Voice operated receive-to-transmit switching. Ptt switching also operable.
NB	Noise blanker.
PROC	Speech processor.
AGC	Receiver automatic gain control.
SLOW	Selects slow AGC action when depressed; fast AGC when out. (AGC switch must be depressed for fast/slow action to be enabled.)
DELAY	Adjustments for transmit-to-receive switching time delay.
CW	Delay between last key-up-action and receive mode.
SSB	Delay between last microphone VOX input and receive mode.
GAIN	Adjusts levels at which receive-to-transmit switching occurs.
VOX	Voice or line audio input signals.
ANTI	Speaker-to-microphone signals.
Frequency readout	Displays frequency in 10-Hz increments.

Table 1-1. Front Panel Controls and Indicators (Cont).

ITEM	FUNCTION
Frequency control switches	Selects frequency increments affected by tuning knob. Continuous tuning for any increment with roll-around at end limits.
⌐¬	1-MHz increments.
SYNC	Loads displayed frequency in nonselected vfo register to synchronize both vfo frequencies.
LOCK	Dial lock prevents tuning knob from changing frequency when rotated.
|	1-kHz increments.
⌐ (left)	100-Hz increments.
¬ (right)	10-Hz increments.
POWER	Primary power switch.
Tuning knob	Frequency selection control. (Provides 200 increments per revolution for all except MHz steps at 20 increments per revolution.) Works in conjunction with switches above knob.
SPOT	In CW mode only, enables 800-Hz tone to which received CW tone is matched to spot transmitted frequency to exact received frequency.
VFO	Selects frequency-storage register.
A	A register. Transmit and receive on same frequency.
B	B register. Transmit and receive on same frequency.
RA-TB	Receive on A register frequency-transmit on B register frequency.
RB-TA	Receive on B register frequency-transmit on A register frequency.
SELECTIVITY	Controls selectivity of receiver.
PBT (small knob)	Passband tuning. Used to select USB, LSB, or CW during receive mode. Continuously varies position of passband (bandwidth selected by BW control) within 8-kHz passband of first if filter.
BW (large knob)	Selects filter bandwidth.

Table 1-1. Front Panel Controls and Indicators (Cont).

ITEM	FUNCTION
8.0	8.0-kHz filter (for AM, also selects optional 6-kHz AM filter if installed).
2.2	2.2-kHz filter (for normal SSB).
OPT 1, 2, 3	Three positions for optional filters.
MODE	Selects mode of transmit operation.
CW	Continuous wave.
USB	Upper sideband. Receive sideband determined by setting of PBT control.
LSB	Lower sideband.
AM RCV	Amplitude modulation in receive only. Transmitter does not operate in AM mode.
GAIN	Adjusts gain of receiver circuits.
AF (small knob)	Af amplifier gain.
RF (large knob)	Rf amplifier gain.
MIC/CARRIER	In sideband operation adjusts microphone amplifier gain. In CW operation adjusts rf carrier level.
PHONES	Output jack for low-impedance (4- to 8-Ω) headphones. Connecting phones inhibits speaker and SPKR (on rear panel) outputs.
MIC	Input jack for low-impedance, dynamic microphone. Jack is also wired for ptt signal. Units with serial numbers 51 and greater are factory wired for a nominal 3-kilohm microphone impedance. Either a low- or high-impedance dynamic microphone may be used without modification of the unit.

1.4 TRANSCEIVER REAR PANEL

Figure 1-2 locates and identifies the connectors on the rear of the transceiver. A brief description of each connector is given in table 1-2. Table 1-3 describes the signal parameters associated with each connector. Figures 1-3 and 1-4 show the interconnection at the rear panel when the transceiver is operating alone and when it is operated with a linear power amplifier such as the 30L-1.

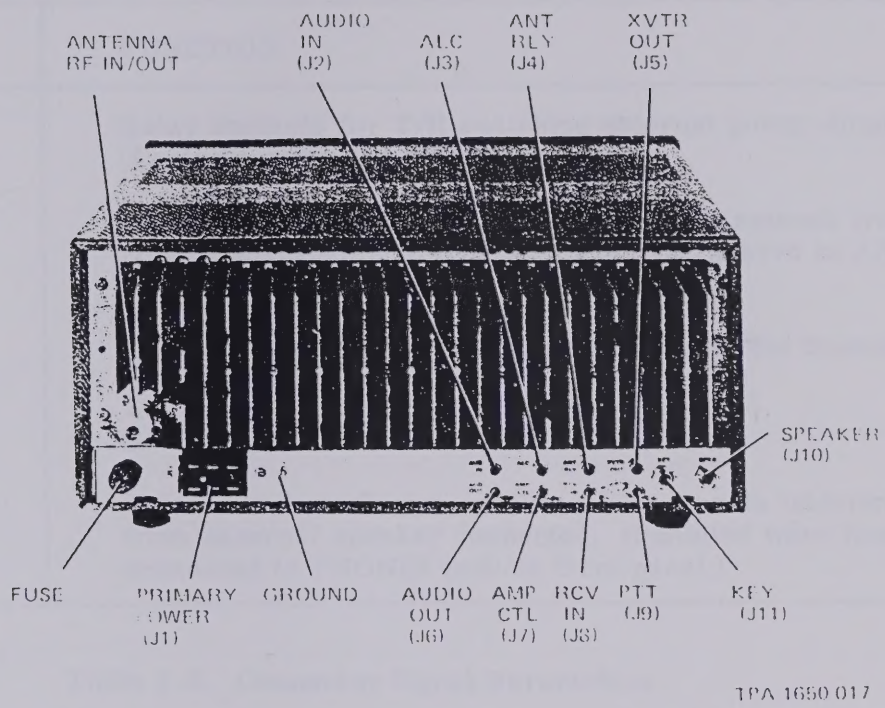


Figure 1-2. Rear Panel Connectors.

ITEM	FUNCTION
Antenna	Rf connector (type SO-239) for coaxial cable connection to antenna coupler.
Fuse	Primary power fuse (8 A for 100 V, 4 A for 220 V).
J1	Primary power connector.
Ground	Stud for earth-ground connection.
AUD IN (J2)	Input for 600-ohm, unbalanced line audio.
ALC (J3)	Negative ALC input signal from external power amplifier.
ANT RLY (J4)	Receive contacts of internal antenna transfer relay. (Jumpered to RCV IN (J8) if seperate receive antenna not used.)
XVTR OUT (J5)	Exciter output signal for use with transmitting converter.
AUD OUT (J6)	Output for 600-ohm, unbalanced line audio.

Table 1-2. Rear Panel Connectors (Cont).

ITEM	FUNCTION
AMP CTL (J7)	Relay contacts for T/R switching external power amplifier. (Contacts grounded in transmit mode.)
RCV IN (J8)	Receiver front end signal input. Bypasses antenna transfer relay and transmit low-pass filters. (Jumpered to ANT RLY (J4) if separate receive antenna not used.)
PTT (J9)	Push-to-talk switch input. Ground to command transmit operation.
KEY (J10)	CW key input.
SPKR (J11)	Output for 4- to 8-ohm speaker. Disconnects internal speaker when external speaker connected. (Inhibited when headphones connected to PHONES jack on front panel.)

Table 1-3. Connector Signal Parameters.

CONNECTOR	SIGNAL PARAMETER
Microphone (mates with PJ-068	Tip--ptt line; ground to transmit. Ring--microphone audio; low-impedance input (270 Ω), approx 5 mV in for full power output. Barrel--common ground.
Headphones (mates with PJ-055)	Tip--receiver audio; 4- to 8-Ω impedance, up to 4-W output. Barrel--ground.
External SPKR (mates with PJ-055)	Tip--receiver audio; 4- to 8-Ω impedance, up to 4-W output. Barrel--ground.
CW KEY (mates with PJ-055)	Tip--keying line; ground to transmit. Barrel--ground.
J2 Line audio in (mates with phono plug)	600 unbalanced; 40-mV input produces 100-W rf output.
J3 ALC (mates with phono plug)	Input for negative ALC voltage from external power amplifier.

Table 1-3. Connector Signal Parameters (Cont).

CONNECTOR	SIGNAL PARAMETER
J4 Antenna relay (mates with phono plug)	External access to receiver contacts of internal antenna transfer relay. Internally jumpered to J8. (Cut jumper if used.)
J5 Transverter (mates with phono plug)	Approximately 200-mW (100-mW, min) output from exciter into 50-ohm load. (To obtain output, connect this line to dc ground through a 1-mH rf choke.)
J6 Line audio out (mates with phono plug)	600 Ω, unbalanced; -10 dB mW at AGC threshold. Level is independent of audio gain control.
J7 Ampl control (mates with phono plug)	Normally open relay contacts; contacts grounded in transmit. 2 A, 28 V dc or 0.75 A, 115 V ac capacity.
J8 Rcvr antenna input (mates with phono plug)	Direct input to receiver front end. Bypasses transmit low-pass filters and antenna transfer relay. Internally jumpered to J4. (Cut jumper if used.)
J9 Push-to-talk (mates with phono plug)	Ground to place transceiver in transmit. (Line is connected to +5 V through 10-kΩ resistor.)

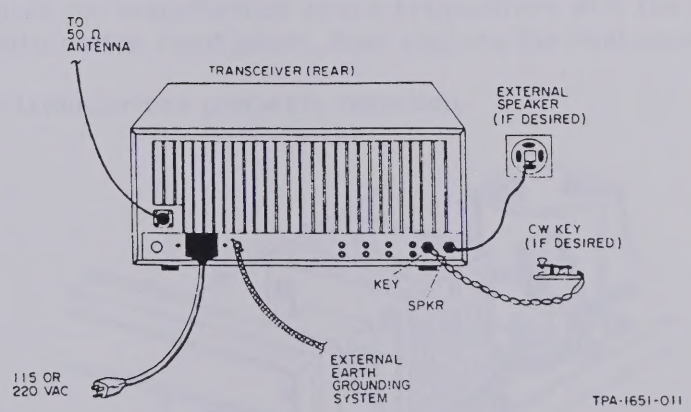


Figure 1-3. Interconnection for Transceiver Alone.

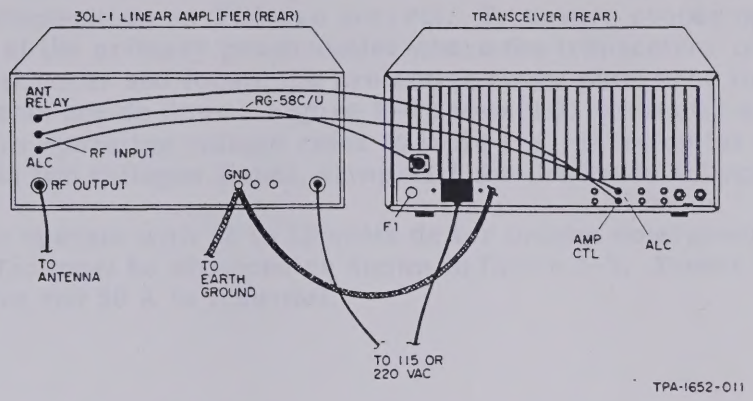


Figure 1-4. Interconnection for Transceiver and Linear Amplifier.

1.5 POWER TRANSFORMER INSTALLATION AND STRAPPING

To eliminate the possibility of the transformer breaking loose from the chassis and causing further damage during shipment, it is packaged separately. The transformer is quickly installed in five steps with just a 3/8-in open-end wrench, no 12 (3/8-in) nutdriver, and a Phillips screwdriver.

a. Using the screwdriver, remove four screws from the bottom of the transceiver (near the rubber feet at each corner) and slide the dust cover off over the heat sink.
b. Remove the front one of the two Phillips-head screws securing the front panel braces to the sides of the chassis and tilt the panel forward.
c. Position the transformer so terminals 1 through 8 face the front panel. With the nutdriver, remove the four nuts and lockwashers from the chassis mounting studs in the right front corner of the chassis and set the transformer over the studs.
d. Using the wrench and nutdriver, secure the transformer to the studs with the four lockwashers and nuts.
e. Electrically connect the transformer to the transceiver with the two attached polarized connectors. Preattach the front panel, then replace the dust cover.

Figure 1-5 shows the transformer properly installed.

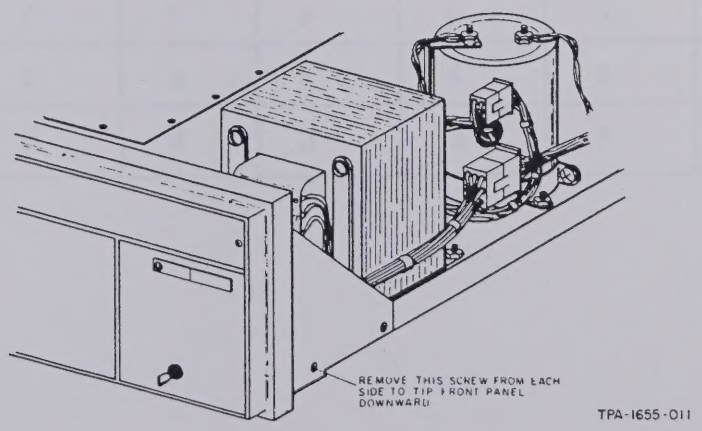


Figure 1-5. Power Transformer Installation.

Because the KWM-380 will operate from various 50- to 60-Hz voltages it is important that the internal strapping connections on TB1 are correct. To ensure proper operation, determine the average ac voltage at the primary power outlet where the transceiver is to be used. Remove the chassis dust cover and locate the protective cover plate near the left rear corner as viewed with the chassis upside down. Figure 1-6 shows TB1 correctly strapped for 105 or 240 volts. For any other operating voltage refer to table 1-4. If the outlet voltage is approximately halfway between two voltages listed, strap TB1 for the lower voltage.

The KWM-380 will also operate with 12 to 15 volts dc for backup emergency power. The primary power connector must be strapped as shown in figure 1-7. Power requirements are nominally 3 A in receive and 20 A in transmit.

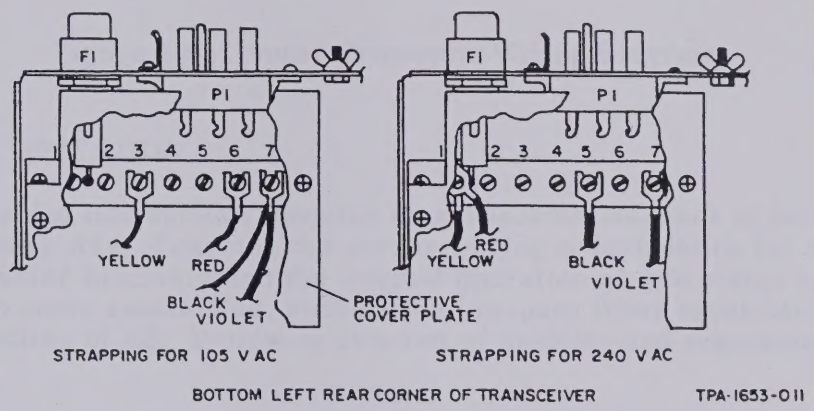


Figure 1-6. AC Input Strapping on TB1.

Table 1-4.

For input voltages listed, strap TB1 as follows:

Wire	105	115	125	210	220	230	240	250
Black	7	7	7	6	6	5	5	4
Yellow	3	2	1	3	2	2	1	1
Red	6	5	4	3	2	2	1	1

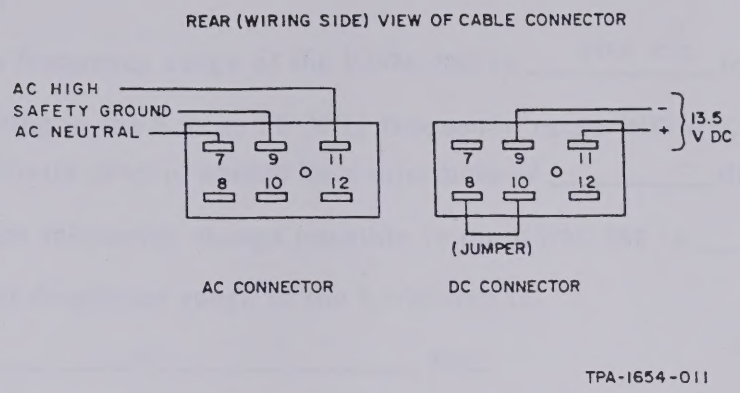


Figure 1-7. Power Connector Wiring Diagram.

1.6 MODULE IDENTIFICATION

The KWM-380 is divided into various modules or subassemblies, each of which is given an A designation, A1 through A14. Learning the corresponding A designation for each of the assemblies will make it easier to understand the overall operation of, and signal tracing through the transceiver. On some assemblies, such as the low-pass filter assembly A2, A2A1 and A2A2 are subassemblies of A2. Following is a list of modules and subassemblies that make up the KWM-380.

A1 Power Amplifier Assembly
A1A1 Power Amplifier
A2 Low-Pass Filter Assembly
A2A1 Low-Pass Filter
A2A2 Directional Coupler/TR Relay
A3 Receiver-Exciter
A4 Passband Tuning
A5 Synthesizer
A6 -(unassigned)-
A7 Oscillator
A8 Control Card
A9 Chassis Assembly
A9A1 Power Supply Control Card
A9A2 +24 V Regulator
A10 Front Panel Assembly
A10A1 Display
A11 Noise Blanker
A12 Speech Processor
A13 Passband Tuning Option
A14 Control Interface

1.7 SELF-TEST

1. The receive frequency range of the KWM-380 is 500 KC to 30 MHz.
2. When operating in the 2.0- to 30-MHz frequency range with a 0.5 μV input signal, the output sensitivity (s+n/n) should be a minimum of _____ dB.
3. The minimum frequency change possible in the KWM-380 is _____ Hz.
4. The transmit frequency range of the KWM-380 is:

   a _____ to _____ MHz

   b _____ to _____ MHz

   c _____ to _____ MHz

   d _____ to _____ MHz

   e _____ to _____ MHz

   f _____ to _____ MHz

5. After a 10 minutes warmup with the 39.6- and 445.-MHz oscillators set to within ±3 Hz, the frequency accuracy of the transceiver is ± _____ kHz.
6. The front panel frequency control switches control _____.
7. When a CW key is used it is connected at J_____ on the rear panel.
8. For 220 V ac operation TB1 is strapped:

   a. yellow wire to pin _____

   b. black wire to pin _____

   c. Red wire to pin _____

9. For dc operation pins _____ and _____ of J1 must be jumpered together.
10. A5 is the designation for the _____ card.

1.8 SELF-TEST ANSWERS

1. 0.5 to 30.0 MHz
2. 10. dB
3. 10 Hz
4. a. 1.800 to 2.000 MHz
   b. 3.500 to 4.000 MHz
   c. 7.000 to 7.300 MHz
   d. 14.000 to 14.350 MHz
   e. 21.000 to 21.450 MHz
   f. 28.000 to 29.700 MHz
5. 5 Hz
6. Frequency Tuning Rate
7. J 1
8. a. 2
   b. 6
   c. 2
9. 8 and 10
10. Synthesizer

2.1 OBJECTIVES

2.2 INTERCONNECT DIAGRAM ANALYSIS

2.1 OBJECTIVES

This section of the manual presents information on the KWM-380 chassis interconnect. At the conclusion of this section the student should have accomplished the following:

a. Be able to trace signals from one module to another through the interconnect diagram.
b. Know what signals or voltages are present on each of the interconnect lines.
c. Know where signals in the interconnect are generated and where they are used.
d. Understand the function and operation of the controls, indicators, inputs and outputs shown on the interconnect diagram.

2.2 INTERCONNECT DIAGRAM ANALYSIS

Refer to the interconnect diagrams, sheets 1 through 5, in the KWM-380 Service Manual. The interconnect diagram shows the interconnections between the modules and subassemblies that make up the KWM-380. The front panel controls, indicators, and input and output connectors, with the exception of the frequency display, are shown on the interconnect diagram. Also shown on the diagram are the rear panel connectors, with the exception of the primary power input and the antenna rf in/out connector.

The following list gives a brief description of each interconnect line, starting at the top of sheet 1, what signals or voltages are present, where the signals originate and where they are used.

Refer to interconnect diagram, sheet 1 in the service manual.

Function:

BCD 4	A8J1/P1-3 to A10J1/P7-4/10. Frequency information, logic 1 or 0, originating in the control board A8, and used in the front panel frequency display A10. Bcd weight 4 information for 10 Hz through 10 MHz display.
BCD 8	A8J1/P1-5 to A10J1/P7-7/8. Frequency information, logic 1 or 0, originating in the control board A8, and used in the front panel frequency display, A10. Bcd weight 8 information for 10 Hz through 10 MHz display.
ADR 1	A8J1/P1-6 to A10J1/P7-10/9. Frequency address information, logic 1 or 0, originating in control board A8, and used in front panel frequency display A10. Address information routes the bcd frequency information to the proper display.
BCD 1	A8J1/P1-7 to A10J1/P7-5/6. Frequency information, logic 1 or 0, originating in control board A8, and used in front panel frequency display A10. Bcd weight 1 frequency information for 10 Hz through 10 MIlz display.

ADR 2	A8J1/P1-8 to A10J1/P7-7/8. Frequency address information, logic 1 or 0, originating in control board A8, and used in front panel frequency display A10. Address information routes the best frequency information to the proper display.
BCD 2	A8J1/P1-9 to A8J1/P7-3/4. Frequency information, logic 1 or 0 originating in control board A8, used in front panel frequency display A10. Bcd weight 1 frequency information for 10 Hz through 10 MIlz display.
ADR 4	A8J1/P1-10 to A10J1/P7-6/5. Frequency address information, logic 1 or 0, originating in control board A8, used in front panel frequency display A10. Address information routes bed frequency information to the proper display.
LPF 2	Not used in KWM-380.
LPF 4	Not used in KWM-380.
LPF 5	Not used in KWM-380.
LPF 7	Not used in KWM-380.
LPF 1	Not used in KWM-380 (KEYWAY).
LPF 8	A8J2/P2-6 to A1A1J1/P27-6. Frequency band information to come low-pass filter number 1. Logic 0 selects 1.6 to 2.0 MHz filter.
LPF 3	A8J2/P2-7 to A2A1J8/P8-7. Frequency band information, logic or 0, originating in A8, used in A2A1. Logic 0 selects 3 to 4 MHz low-pass filter.
LPF 6	A8J2/P2-8 to A2A1J8/P8-8. Frequency band information, logic or 0, originating in A8, used in A2A1. Logic 0 selects 7 to 10MHz low-pass filter
LPF 8	A8J2/P2-9 to A2A1J8/P8-9. Frequency band information, logic or 0, originating in A8, used in A2A1. Logic 0 selects 14 to 20 low-pass filter.
LPF 9	A8J2/P2-10 to A2A1J8/P8-10. Frequency band information, logic 1 or 0, originating in A8, used in A2A1. Logic 0 selects 20 to 3 MHz low-pass filter.
GND	A8J3/P3-1 to A5A2J2/P22-1. Ground between A8 and A5A2.
STROBE	A8J3/P3-2 to A5A2J2/P22-2. Logic 1 or 0, originating in A8, used in A5A2. A logic 0 to 1 transition of the strobe is used to shift serial frequency information to the parallel outputs of the storage registers in the frequency synthesizer.
DATA	A8J3/P3-3 to A5A2J2/P22-3. Serial frequency information, logic 1 or 0, originating in A8, used in A5A2. Contains 10 Hz to 10MHz frequency information.

CLOCK	A8J3/P3-4 to A5A2J2/P22-4. Clock pulse, logic 1 or 0, originating in A8, used in A5A2. Used to clock serial frequency data into shift/storage registers.
SPARE	Not currently used.
SPARE	Not currently used.
SPARE	Not currently used.
SPARE	Not currently used.
PAD R1	A8J4/P4-1 to A14P1-1. Row 1 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in control board A8.
PAD R2	A8J4/P4-2 to A14P1-2. Row 2 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in control board A8.
PAD R3	A8J4/P4-3 to A14P1-3. Row 3 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in control board A8.
PAD R4	A8J4/P4-4 to A14P1-4. Row 4 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in control board A8.
PAD C1	A8J4/P4-5 to A14P1-5. Column 1 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in control board A8.
PAD C2	A8J4/P4-6 to A14P1-6. Column 2 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in A8.
PAD C3	A8J4/P4-7 to A14P1-7. Column 3 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in A8.
PAD C4	A8J4/P4-8 to A14P1-8. Column 4 information from a remote 16-key pad with a code that is 2-out-of-8. Logic 1 or 0 information used in A8.
+5 V dc	A8J4/P4-9 to A14P1-9. +5 V dc from A8 to A14 to supply remote key pad.
GND	A8J4/P4-10 to A14P1-10. Ground between A8 and A14.
STROBE	A8J4/P4-11 to A14P1-11. Logic 1 or 0 output from A8 to A14 for use with remote frequency information.
10's	A8J4/P4-12 to A14P1-12. 10 MHz, weight 2 frequency information. Logic 1 or 0, originating in A8, available at A14 for remote use.

10's	A8J4/P4-13 toA14P1-13. 10 MHz, weight 1 frequency information. Logic 1 or 0, originating in A8. available at A14 for remote use.
1's	A8J4/P4-14 to A14P1-14. 1 MHz, weight 8 frequency information. Logic 1 or 0, originating in A8, available at A14 for remote use.
1's	A8J4/P4-15 to A14P1-15. 1 MHz, weight 4 frequency information. Logic 1 or 0, originating in A8, available at A14 for remote use.
1's	A8J4/P4-16 to A14P1-16. 1 MHz, weight 2 frequency information. Logic 1 or 0, originating in A8, available at A14 for remote use.
1's	A8J4/P4-17 to A14P1-17. 1 MHz, weight 1, frequency information. Logic 1 or 0, originating in A8 available at A14 for remote use.
SPARE	Not used.
REMOTE	A8J4/P4-19 to A14P1-19. +5 V dc to A8 from remote control interface to keep microprocessor alive while operating with remote control.
SPARE	Not used.
SPARE	Not used.
SPARE	Not used.
	A8J5/P5-3 to A3J13/P13-35. Frequency band information. Logic 1 or 0. Logic 1 with 7 to 10 MHz operation. Originating in A8, used in A3.
B8	A8J5/P5-4 to A3J13/P13-36. Frequency band information. Logic 1 or 0. Logic 1 with 14 to 20 MHz operation. Originates in A8, used in A3.
B9	A8J5/P5-5 to A3J13/P13-37. Frequency band information. Logic 1 or 0. Logic 1 with 20 to 30 MHz operation. Originates in A8, used in A3.
CTTL	A8J5/P5-6 to A3J13/P13-39. Transmit inhibit. Logic 1 or 0. Logic 1 to inhibit transmit operation when a frequency not in the ham bands is selected.
GND	A8J5/P5-8 to A3J13/P13-40. Ground between A3 and A8.
ENCODER A	A6J6/P6-1 to G1-A. One of two outputs from the front panel frequency tuning encoder. Logic 1 or 0. Used in A8 to determine speed and rotation of frequency tuning knob.
ENCODER B	A6J6/P6-2 to G1-B. One of two output from the front panel frequency tuning encoder. Logic 1 or 0. Information used in A8 to determine speed and rotation of frequency tuning knob.

VFO SELECT	A6J6/P6-3 to 53-1. Logic 1 or 0 from front panel VFO SELECT knob. Logic 1 with A register selected, logic 0 with B register selected.
SYNC	A6J6/P6-5 to S6B. Logic 1 or 0 from front panel SYNC button. Logic 1 used in A8 to load displayed frequency in nonselected vfo register to synchronize both vfo frequencies.
SPARE	Not used.
1 MHz SELECT	A6J6/P6-7 to S6A-1. Logic 1 or 0 from front panel ⌐¬ switch. Logic 1 with button depressed. Used in A8 to cause 1 MHz tuning increments when tuning knob is rotated.
1 kHz SELECT	A6J6/P6-8 to S6D-1. Logic 1 or 0 from front panel | switch. Logic 1 with button depressed. Used in A8 to cause 1 kHz tuning increments when tuning knob is rotated.
100 Hz SELECT	A6J6/P6-9 to S6E-1. Logic 1 or 0 from front panel ⌐ (left) switch. Logic 1 with button depressed. Used in A8 to cause 100 Hz tuning increments when tuning knob is rotated.
10 Hz SELECT	A6J6/P6-10 to S6F. Logic 1 or 0 from front panel ⌐ (right) switch. Logic 1 with button depressed. Used in A8 to cause 10 Hz tuning increments when tuning knob is rotated.
SPARE	Not used.
GND	A6J6/P6-13 to GND. Ground connection between A6 and frequency tuning encoder.
+5 V dc	A6J6/P6-14 to G1 +5V. +5 V from A6 used in frequency tuning encoder.
	Refer to interconnect schematic sheet 2.
+24 V dc	A5A2J1/P9-1 to A3J13/P13-1. +24 V dc supplied from A3 to A5A2.
+5 V dc	A5A2J1/P9-2 to A3J13/P13-2. +5 V dc supplied from A3 to A5A2.
+9 V dc	A5A2J1/P9-3 to A3J13/P13-3. +9 V dc supplied from A3 toA5A2.
GND	A5A2J1/P9-4 to A3J13/P13-4. Ground between A5A2 and A3.
GND	A5A2J1/P9-5 to A3J13/P13-5. Ground between A5A2 and A3.
LOL	A5A2J1/P9-6 to A3J13/P13-6. Logic 1 or 0 output from the synthesizer, used in A3. Logic 0 indicates a loss of lock (fault) in the synthesizer.
+14 V dc	A7J1/P10-1 to A3J13/P13-8. +14 V dc from A3 to oscillator assembly A7.
SPARE	Not used.

+5 V dc	A7J10/P10-3 to A3J13/P13-9. +5 V dc from A3 to oscillator assembly A7.
_W OSC KEYING	A7J1/P10-4 to A3J13/P13-10. Logic 1 or 0 from A3 to A7. Logic 1 enables 455 kHz bfo output from A7.
+9 V dc	A7J1/P10-5 to A3J13/P13-11. +9 V dc from A3 to A7.
455 kHz ENABLE	A7J1/P10-6 to A3J13/P13-12. Logic 1 or 0 from A3 to A7. Logic 1 enables 455 kHz bfo.
GND	A7J1/P10-7 to A3J13/P13-13. Ground between A3 and A7.
454.2 kHz ENABLE	A7J1/P10-8 to A3J13/P13-14. Logic 1 or 0 from A3 to A7. Used to enable 454.2 kHz bfo on A7 module.
SPARE	Not used.
SPARE	Not used.
SPARE	Not used.
SPARE	Not used.
+24 V dc	A3J13/P13-19 to A4J1/P11-3. +24 V dc from A3, used in A4.
+5 V dc	A3J13/P13-20 to A4J1/P11-4. +5 V dc from A3, used in A4.
4 V dc	A3J13/P13-21 to A4J1/P11-5. +14 V dc from A3, used in A4.
GND	A3J13/P13-22 to A4J1/P11-6. Ground between A4 and A3.
+9 V dc	A3J13/P13-23 to A4J1/P11-7. +9 V dc from A3, used in A4.
8 kHz FLTR SEL	A3J13/P13-24 to A4J1/P11-8. Logic 1 or 0 from A3, used in A4. Logic 1 selects FL3 (AM PASSBAND FILTER) on A4.
OPT 3 FLTR SEL	A13P13-25 to A4J1/P11-9. Logic 1 or 0 from A3, used in A4. Logic 1 selects optional filter FL4 (CW NARROW PASSBAND FILTER) on A4.
USB XMT	A3J13/P13-26 to A4J1/P11-10. Logic 1 or 0 from A3, used in A4. Logic 1 sets A4 oscillator for upper sideband operation.
OPT 2 FLTR SEL	A3J13/P13-27 to A4J1/P11-11. Logic 1 or 0 from A3, used in A4. Logic 1 selects FL2 (CW WIDE PASSBAND FILTER) on A4.
LSB XMT	A3J13/P13-28 to A4J1/P11-12. Logic 1 or 0 from A3, used in A4. Logic 1 sets A4 oscillator for lower sideband operation.
2.2 kHz FLTR SEL	A3J13/P13-29 to A4J1/P11-13. Logic 1 or 0 from A3, used in A4. Logic 1 select FL1 (SSB WIDE PASSBAND FILTER).
" XMT	A3J13/P13-30 to A4J1/P11-14. Logic 1 or 0 from A3, used in A4. Logic 1 sets A4 oscillator for CW operation.

OPT 1 FLTR SEL	A3J13/P13-31 to A4J1/P11-15. Logic 1 or 0 from A3, used in A4. Logic 1 selects optional filter FL5 (SINGLE SIDEBAND NARROW PASSBAND FILTER)
$\overline{\text{PTT}}$	A3J13/P13-32 to A4J1/P11-16. Logic 1 or 0 from A3, used in A4. Logic 1 enables PBT (small knob) on front panel during receive operation.
PBT CONT LOW	ANJ7 to front panel PBT control. Low side of PBT variable resistor.
PBT CONT ARM	A4J8 to front panel PBT control. Wiper on PBT variable resistor.
PBT CONT HIGH	A4J9 to front panel PBT control. High side of PBT variable resistor.
BW-8	A3J12/P12-1 to S8, front panel BW filter select switch. +9 V dc from BW (large knob) switch S8 to A3 with 8.0 selected in receive operation.
BW-2.2	A3J12/P12-2 to S8, front panel BW filter select switch. +9 V dc from BW (large knob) switch S8 to A3 with 2.2 selected in receive operation.
BW-OPT 1	A3J12/P12-3 to S8, front panel BW filter select switch. +9 V dc from BW (large knob) switch S8 to A3 with bandwidth option 1 selected in receive operation.
BW-OPT 2	A3J12/P12-4 to S8, front panel BW filter select switch. +9 V dc from BW (large knob) switch S8 to A3 with bandwidth option 2 selected in receive operation.
BW-OPT 3	A3J12/P12-5 to S8, front panel BW filter select switch. +9 V dc from BW (large knob) switch S8 to A3 with bandwidth option 3 selected in receive operation.
+9.V RCV	A3J12/P12-6 to S8, front panel BW filter select switch. +9 V dc from A3 to front panel BW switch during receive operation.
MODE-LSB	A3J12/P12-7 to S4, front panel MODE select switch. +5 V dc from S4 to A3 with LSB selected on MODE switch.
MODE-CW	A3J12/P12-8 to S4, front panel MODE select switch. +5 V dc from S4 to A3 with CW selected on MODE switch.
MODE-AM	A3J12/P12-9 to S4, front panel MODE select switch. +5 V dc from S4 to A3 with AM RCV selected on MODE switch.
MODE USB	A3J12/P12-10 to S4, front panel MODE select switch. +5 V dc from S4 to A3 with USB selected on MODE switch.
$\overline{\text{PTT}}$	A3J12/P12-11 to S7A, front panel MOX switch and S7B front panel VOX switch. Logic 1 or 0. Logic 0 with front panel MOX switch depressed. Logic 0 with front panel VOX switch depressed and a logic 0 output from VOX circuit. Logic 0 into A3 is used to key radio.

VOX OUT	A3J12/P12-12 to S7B, front panel VOX switch. Logic 1 or 0. Logic 0 output from A3 with key output from VOX circuit.
NB ENBL	A3J12/P12-13 to S7C, front panel NB switch. +9 V dc from S7C to A3 with NB (noise blanker) switch depressed.
PROC ENBL	A3J12/P12-14 to S7D, front panel PROC switch. +9 V dc from S7D to A3 with PROC (processor) switch depressed.
AGC OFF	A3J12/P12-15 to S7E, front panel AGC switch. +5 V dc from S7E to A3 with AGC (automatic gain control) switch not depressed. With switch depressed (AGC on) 0 V applied to A3.
AGC SLOW	A3J12/P12-16 to S7F, front panel SLOW switch. +5 V dc from S7F to A3 with SLOW switch not depressed, 0 V dc, slow AGC action, with switch depressed.
PTT	A3J12/P12-17 to S3, front panel VFO select switch. Logic 1 or 0. Logic 1 with PTT (push-to-talk) signal present.
$\overline{\text{SPOT}}$	A3J12/P12-80 to S2, front panel SPOT switch. Logic 1 or 0. Logic 0 with spot button depressed (spot circuits activated).
+5 V dc	A3J12/P12-19 to S7E, front panel AGC switch. Provides +5 V dc to S7E.
VOX A	A3J15/16-S to S7B output from front panel VOX switch to U910A on A3.
VOX B	A3J15/P15-6 to S7B input to front panel VOX switch from U913A on A3. Input is logic 1 with CW selected and key down.
	Refer to schematic sheet 3.
SAFETY GND -12 V dc	A9J1-9 to ground.
115/230 V ac (H) or +V dc	A9J1-11 to TB1-X. Primary power path through on-off switch and fuse F1.
115/230 V ac (L) and FAN AC	A9J1-7 to P2-9. 115/230 V ac return through on-off switch.
FAN AC	A9J1-12 to P2-6. Ac power from chassis to operate external cooling fan.
+12 V dc to JUMPER	A9J1-10 to TB1-X. +12 V dc to TB1 through fuse F2.
+12 V dc from JUMPER	A9J1-8 to VR2. +12 V dc from jumper on A9 chassis.
PWR GND	A3J14/P14-1 to A9A2-E4. Ground connection between chassis and A3 module.
+24 V dc	A3J14/P14-3 to A9A2-E3. +24 V dc from power supply to A3.

+5 V dc	A3J14/P14-5 to A9A1-E2. +5 V dc from power supply to A3.
+5 V dc	A3J14/P14-6 to A9A1-E3. +5 V dc from power supply to A3.
+9 V dc	A3J14/P14-10 to A9A1-E7. +9 V dc from power supply to A3.
GND	A3J14/P14-11 to A9A1-E4. Ground between power supply and A3.
GND	A3J14/P14-12 to A9A1-E5. Ground between power supply and A3.
+14 V dc AUDIO PA/OVEN	A3J14/P14-13 to A9A1-E12. +14 V dc from power supply to A3.
+14 V dc	A3J14/P14-14 to A9A1-E10. +14 V dc from power supply to A3.
+14 V dc (high I)	A1A1J2 to VR2. +14 V dc high current from the cathode of VR2 in the power supply to the power amplifier.
PWR GND	A1A1J3 to VR2. Ground connection between the anode of VR2 in the power supply and the power amplifier.
CARR LOW	A3J15/P15-1 to R6A, front panel MIC/CARRIER adjust. Low side, terminal 1, of MIC/CARRIER adjust variable resistor R6A.
CARR ARM	A3J15/P15-2 to R6A, front panel MIC/CARRIER adjust. Wiper, terminal 2, of MIC/CARRIER adjust variable resistor R6A.
CARR HIGH	A3J15/P15-3 to R6A, front panel MIC/CARRIER adjust. High side, terminal 3, of MIC/CARRIER adjust variable resistor R6A.
RF LOW	A3J15/P15-7 to R5A, front panel GAIN control. Low side, terminal 3, of RF GAIN control variable resistor R5A.
RF HIGH	A3J15/P15-8 to R5A, front panel GAIN control. High side, terminals 1 and 2 of RF GAIN control variable resistor R5A.
MTR-	A3J15/P15-10 to M1, front panel meter. Low or - input to front panel meter.
MTR +	A3J15/P15-11 to M1, front panel meter. High or + input to front panel meter.
MTR(PF)	A3J15/P15-12 to SS, front panel METER switch. Positive dc voltage (forward power analog) adjustable in A3 for proper meter indication.
MTR(VC)	A3J15/P15-13 to S5-3. Collector voltage sample from A3 to front panel meter switch.
MTR COMMON	A3J15/P15-14 to S5, front panel meter switch. Output from S5 to A3 may contain MTR(VC), MTR(PF), MTR(ALC), or MTR(PR) voltage depending on METER switch setting.

MTR(ALC)	A3J15/P15-15 to S5, front panel meter switch. Positive dc analog voltage of automatic level control from A3 to METER switch. Voltage varies as ALC varies.
MTR(PR)	A3J15/P15-16 to S5, front panel METER switch. Positive dc analog voltage of reflected power, from A3 to METER switch. Voltage varies as reflected power varies.
XMT MONITOR	A3J16/P16-1 to A1A1J3/P21-6. Logic 1 or 0. Logic 0 output from A1A1 to A3 with 50 watts or greater rf output from the pa.
PWR MTR	A3J16/P16-2 to A1A1J3/P21-16. Positive dc analog voltage directly proportional to pa rf output power, developed in A1A1, routed to A3.
+9 V XMT	A3J16/P16-3 to A1A1J3/P21-7. +9 V dc or 0 V dc, from A3 to A1A1. +9 V present during transmit operation.
$\overline{\text{AVG ALC INHIBIT}}$	A3J16/P16-4 to A1A1J3/P21-17. Logic 1 or 0. Logic 0, from A3 to A1A1, to inhibit average ALC amplifier in A1A1.
TUNE PWR	Not used.
ALC	A3J16/P16-6 to A1A1J3/P21-18. Positive dc automatic level control voltage. Output of ALC circuits in A1A1. ALC voltage increases to reduce pa output power.
+9 V dc	A3J16/P16-7 to A1A1J3/P21-9. +9 V dc from A3, used in A1A1.
REFL PWR DET	A3J16/P16-8 to A1A1J3/P21-19. Positive dc voltage proportional to reflected power, from A1A1 to A3.
SPARE	Not used.
LINE AUDIO OUT	A3J16/P16-11 to J6, rear panel AUD OUT. 600-ohm audio output from receiver. -10-dB mW into a 600-ohm load.
AMPL CONT	A3J16/P16-12 to J7, rear panel AMP CTL. Relay contact from A3, used for T/R switching an external power amplifier. Contacts grounded in transmit mode.
$\overline{\text{PTT}}$	A3J16/P16-13 to J9, rear panel PTT. Push to talk switch input, from rear panel to A3. Ground at input J9 commands transmit operation.
ALC(AMPL)	A3J16/P16-14 to J3, rear panel ALC. Negative ALC input from an external power amplifier. To reduce rf output power -dc voltage goes more negative.
$\overline{\text{KEY}}$	A3J16/P16-15 to J10, rear panel KEY. CW key input; ground to A3 with key down.
RCVR MUTE	Not used.

PROC ENABLE	A12-1 to A3J17/P17-1. Logic 1 or 0 from A3 to A12, logic 1 with processor enabled.
GND	A12-2 to A3J17/P17-2 ground between A3 and A12.
+14 V dc	A12-3 to A3J17/P17-3. +14 V dc from A3 to A12.
+5 V dc	No connection.
+9 V dc	No connection.
NB ENABLE	A11-E2 to A3J18/P18-1. +9 V dc from A3 to A11 with noise blanker enabled, 0 V dc with noise blanker disabled.
+9 V dc	A11-E3 to A3J18/P18-2. +9 V dc from A3 to A11.
GND	A11-E1 to A3J18/P18-3. Ground connection between A3 and A11.
	Refer to schematic sheet 4.
VOX GAIN	A3J19/P19-1 to R1, front panel VOX gain control. Wiper, terminal 2, of variable resistor used to adjust gain of VOX audio amplifier.
VOX DELAY COM	A3J19/P19-2 to R3 and R4, front panel VOX DELAY control. Output from R3, terminal 2, or R4, terminal 2, depending on mode of operation.
ANTI VOX GAIN	A3J19/P19-3 to R2, front panel ANTI VOX GAIN control. Wiper, terminal 2, of ANTI VOX GAIN control resistor R2, adjusts gain of anti VOX audio amplifier.
CW DELAY	A3J19/P19-4 to R3, front panel CW DELAY control. Terminal 1 of variable resistor R3, enabled during CW operation.
ANTI VOX GAIN	A3J19/P19-5 to R2, front panel ANTI VOX GAIN control. Terminal 3 of variable resistor R2. R2 adjusts gain of anti VOX audio amplifier.
VOX GAIN	A3J19/P19-7 to R1, front panel VOX GAIN control. Terminal 3 of variable resistor R1. R1 adjusts gain of VOX gain amplifier.
SSB DELAY	A3J19/P19-8 to R4, front panel SSB DELAY control. Terminal 1 of variable resistor R4, enabled during SSB operation.
$\overline{\text{TUNE}}$	A3J20/P20-1 to A14P2-1. Logic 1 or 0. Logic 0 from A14 to A3 if external pa or coupler is in a tune cycle. Logic 1 with external pa or coupler tuned or with no external pa or coupler installed.
$\overline{\text{TF}}$	A3J20/P20-2 to A14P2-2. Logic 1 or 0. Logic 0 from A14 to A3 with a fault from an external pa or coupler. Logic 1 with no fault from an external pa or coupler or with no external pa or coupler installed.

$\overline{KI}$	A3J20/P20-3 to A14P1-3. Logic 1 or 0. Logic 0 from A4 to A3 with key interlock present in external equipment. Logic 1 with no key interlock from external equipment or no external equipment used.
$\overline{KEY}$	A3J20/P20-4 to A14P2-4. Logic 1 or 0. Logic 0 from A14 to A3 with key present from external equipment. Logic 1 with no key from external equipment or no external equipment installed.
TUNE PWR	A3J20/P20-6 to A14J2-6.
	Reserved for future use.
SPARE	Not used.
SPARE	Not used.
SPARE	Not used.
SPARE	Not used.
+14 V dc	A1A1J3/P21-1 to A9-E1. +14 V dc from power supply to power amplifier.
+14 V dc	A1A1J3/P21-2 to A9-E1. +14 V dc from power supply to power amplifier.
GND	A1A1J3/P21-3 to TB4-3 ground between TB4 and power amplifier
+14 V dc	A1A1J3/P24-4 to A2A2J24/P24-6. +14 V dc from A1A1 to A2A2.
+9 V XMT	A1A1J3/P21-5 to A2A2J24/P24-7. +9 V dc from A1A1 to A2A2 present during transmit operation.
+14 V dc	A1A1J3/P21-11 to A9-E1. +14 V dc from power supply to power amplifier.
GND	A1A1J3/P21-12 to TB4-3. Ground between TB4 and power amplii
ALC GND	A1A1J3/P21-13 to A2A2J24/P24-1. Automatic level control grou between A1A1 and A2A2.
REF PWR DET	A1A1J3/P21-14 to A2A2J24/P24-2. Positive dc voltage, proportional to reflected power, from A2A2 to A1A1.
FWD PWR DET	A1A1J3/P21-15 to A2A2J24/P24-3. Positive dc voltage, proportional to forward power, from A2A2 to A1A1.
GND	A4J1/P11-3 to A13J3/P26-1. Ground between A4 and A13.
+5 V dc	A4J1/P11-2 to A13J3/P26-2/4. +5 V dc from A4 to A13.
SPARE	

OPT 1 FLTR SEL	A4J3/P11-6 to A13J3/P26-4/6. Logic 1 or 0. Logic 1, from A4 to A13, selects optional filter number 2, narrow, single sideband, passband filter.
+14 V dc	A4J3/P11-7 to A13J3/P26-5/7. +14 V dc from A4 to A13.
OPT 3 FLTR SEL	A4J3/P11-6 to A13J3/P26-6/8. Logic 1 or 0. Logic 1, from A4 to A13, selects optional filter number 3, narrow, CW, passband filter.
SPKR OUT	A3J19/P19-J29 to J11, JS1 and J1. Audio output from A3 to speaker, speaker jack, and headphone jack.
SPKR RTN	A3J19/P19-J30 to audio out common.
MIC IN GND	A3J25 to J2, front panel MIC jack. Ground between MIC input jack and A3.
MIC IN HIGH	A3J24 to J2, front panel MIC jack. Audio input line from MIC jack to A3.
MIC GAIN LOW	A3J28 to R6B, front panel MIC GAIN control. Ground side of MIC gain resistor R6B, terminal 1.
MIC GAIN ARM	A3J27 to R6B, front panel MIC GAIN control. Output, wiper (terminal 2) of MIC GAIN resistor R6B.
MIC GAIN HIGH	A3J26 to R6B, front panel MIC GAIN control. Audio input to R6B, terminal 3, from mic preamp in A3.
MIC GAIN LOW	A3J33 to R5B, front panel AF GAIN control. Ground, terminal 1, of variable resistor R5B.
MIC GAIN ARM	A3J32 to R5B, front panel AF GAIN control. Wiper, terminal 2, of R5B, audio output from variable resistor to output audio amplifier.
AF GAIN HIGH	A3J31 to R5B, front panel AF GAIN control. Audio input, terminal 3, of variable resistor R5B.
LINE AUDIO IN	A3J21 to A9-J2. Line audio in from the rear panel to A3.
LINE AUDIO IN GND	A3J22 to audio in common.
+5 V dc	A8J1/P1-J8 to A9P4. +5 V dc from power supply to control board A8.
GND	A8J1/P1-J7 to A9P5. Ground connection between chassis and A8.
	Refer to schematic sheet 5.
RF to PA	A3J1 to A1A1P1. Rf output from the receiver-exciter to the power amplifier.

PA RF OUT	A1A1P2 to A2A2J1. Rf output from the power amplifier input to the directional coupler.
RF TO/FROM ANT	A2A1J4 to A2A2J2. Transmit rf output from the directional coupler to the antenna or receive rf input from the antenna to the directional coupler.
RCV RF	A2A2P1 to A9J4 and A9J8. Receive signal from T/R relay on A1A1 to J4 and through jumper to J8. With a common receive/transmit antenna jumper between J4 and J8 must be installed, with a separate receive antenna the jumper is removed.
RCV RF IN	A3J9 to A9J8. Receive rf into A3 from separate receive antenna at J8 or through jumper with common antenna.
XVTR OUT	A3J8 to A9J5. Exciter output from A3 to rear panel.
455 kHz IN	A3J6 to A4J3. 455 kHz output from receiver/exciter to passband tuning circuit.
455 kHz OUT	A3J7 to A4J6. 455 kHz output from A4 to A3.
PBT RF IN	A4J4 to A13J2. Rf output from A4 to optional passband tuning circuit A13.
PBT RF OUT	A4J5 to A3J1. Output from optional passband tuning circuit A13 to A4.
NB RF IN	A3J4 to A11P1. Rf input to noise blanker A11 from A3.
NB RF OUT	A3J5 to A11P2. Rf output from noise blanker to A3.
39.6 MHz (to RCVR)	A7P1 to A3J3. 39.6 MHz from oscillator A7 to receiver/exciter A3.
455 kHz	A7P2 to A3J10. 455 kHz from oscillator A7 to A3.
454.2 kHz	A7P3 to A3J11. 454.2 kHz from oscillator A7 to A3.
39.6 MHz (to SYNTH)	A7J2 to A5A2P3. 39.6 MHz reference frequency from A7 to synthesizer A5.
9.9 MHz	A8J9 to A5A2P5. 9.9 MHz from the frequency synthesizer to control board A8, used to develop clock for microprocessor circuits.
100 kHz	A5A1J3 to A5A2P3. 100 kHz from fixed divider in A5A2 to frequency-phase detector in A5A1.
VAR REF	A5A1J2 to A5A2P4. 2.945 to 3.94499 MHz from A5A2 to A5A1.
39.645-69.145 MHz INJ	A5A1P1 to A3J2. Variable injection output of the frequency synthesizer used in the first receive mixer and second transmit mixer on A3.

VOICE SIGNAL IN	A3J26 to A12P26. Voice input to speech processor A12 from A3.
GND (shield)	A3J28 to A12P28 shield for voice audio to speech processor.
VOICE SIGNAL OUT	A12J26 to A10R508-3. Audio output from processor to front panel mic gain control R508.
LOW (shield)	A12J28 to R508-1. Common for audio output line from processor.

3.1 OBJECTIVES

3.2 BLOCK DIAGRAM ANALYSIS

Figure 3-1

3.3 RECEIVE SIGNAL PATH

3.3.1 Low-Pass Filter Assembly A2

Figure 3-2

3.3.2 Receiver-Exciter A3

Figures 3-3 and 3-9

3.3.3 Noise Blank A11

Figure 3-4

3.3.4 Second Receive Mixer

3.3.5 Bandpass Tuning Circuit A4

Figure 3-5
Figure 3-6
Figure 3-7

3.3.6 IF Amplifiers, Detectors, and Audio Output A3

3.3.7 Receive AGC Circuits and Switching Circuits

Figure 3-8
Figure 3-9

3.4 SELF-TEST

3.5 SELF-TEST ANSWERS

3.1 OBJECTIVES

This section of the manual presents an overall view and detailed circuit theory of the circuits involved in the receive signal path. At the conclusion of this section, the student should have accomplished the following:

a. Know the assemblies involved in the receive signal path.
b. Be able to trace the signal through the receive circuits.
c. Understand the operation of the circuits.
d. Be thoroughly familiar with the location of each circuit.

3.2 BLOCK DIAGRAM ANALYSIS

Refer to the KWM-380 simplified block diagram, figure 3-1. The receive signal, entering the transceiver at the antenna RF IN/OUT jack, is routed through the following assemblies before being applied to the speaker.

a. A2 Low-Pass Filter Assembly
b. A3 Receiver-Exciter
c. A4 Passband Tuning
d. A11 Noise Blanker (optional)

The receiver signal enters the transceiver at the antenna jack and is routed through the directional coupler (A2A2) to the low pass filter (A2A1). From this point the signal leaves A2A1 and returns to A2A2 where the T/R relay is located. From the T/R relay the signal is applied to the receiver-exciter board A3. After the first mixer on the receiver-exciter the signal leaves A3 and enters the noise blanker (NB) A11, where high-frequency noise pulses are removed from the signal before it returns to A3. At the output of the second receiver mixer, the signal leaves A3 and enters the passband tuning circuit (PBT) A4. In the passband tuning assembly, the center frequency can be increased or decreased slightly before it is applied to the bandpass filters to reduce adjacent signal interference.

After the signal is filtered in A4, it returns to the receiver-exciter board A3 where it is routed to the AM or product detector. The output of the detector being used is filtered, amplified, and output to the speaker or the 600-ohm unbalanced audio out (J6) at the rear of the transceiver. The receiver-exciter board A3 also contains the receiver automatic gain control (AGC) circuits and the logic circuits that control the switching and signal routing through A3.

The power supply, providing power to the receive circuits, the synthesizer providing the injection frequencies and the control board are discussed in other sections of this manual.

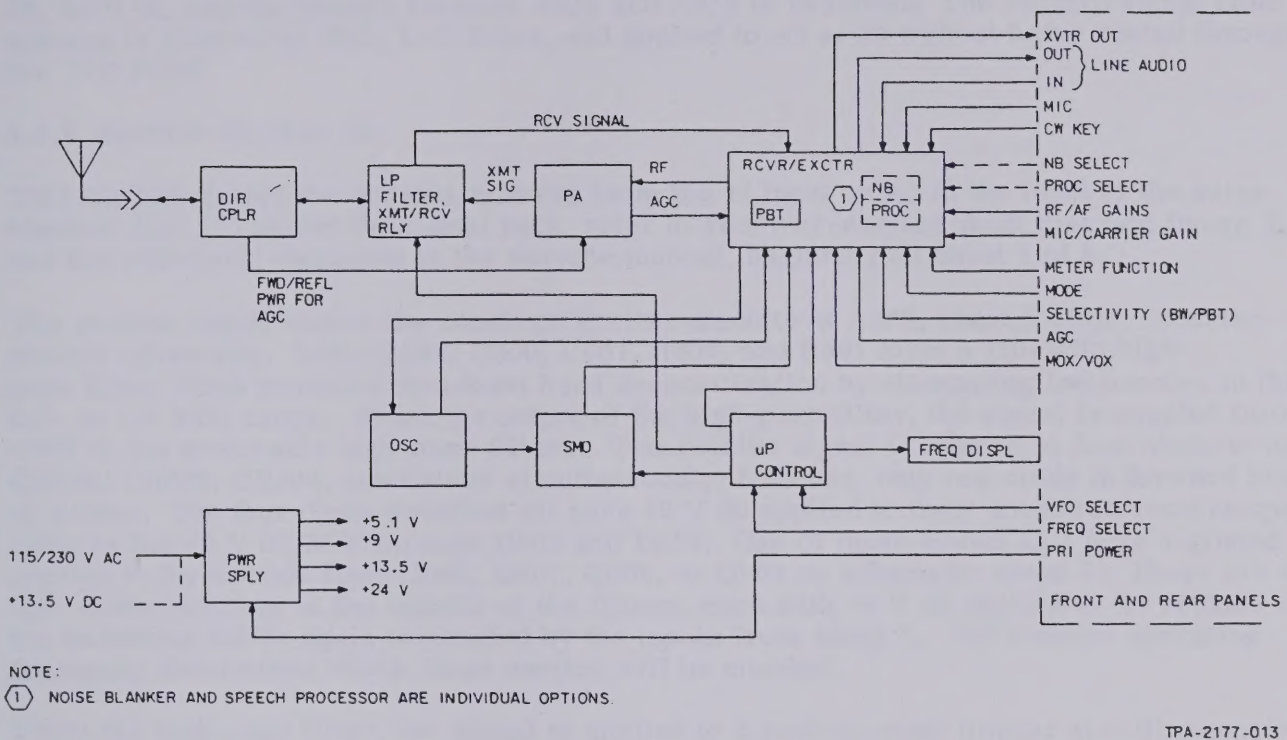


Figure 3-1. KWM-380 Simplified Block Diagram.

3.3 DETAILED RECEIVE SIGNAL PATH THEORY

The receive signal is routed through four assemblies in the KWM-380, the low-pass filter assembly (A2), receiver-exciter board A3, noise blanker (optional) A11, and passband tuning A4.

3.3.1 Low-Pass Filter Assembly A2

Refer to figure 3-2, block diagram of the low-pass filter assembly, and the schematic diagram of A2, found in the KWM-380 Service Manual. When a common receive-transmit antenna is used, the receive signal from the antenna enters the KWM-380 at the antenna RF IN/OUT jack on the back of the unit. From the antenna jack the signal is applied to A2A2J2 on the low-pass filter assembly. The receiver signal passes through T1, part of the forward and reflected power detector, and is applied to A2A1 E9. At the input of A2A1 the signal is applied to relays K7 through K11. The state of the relays determines which filter section will be used for a particular receive frequency. Only one of these relays, on the input of the low-pass filter sections, will be energized at a time. The band information on J1 of A2A1 that energizes the input relay also energizes the corresponding relay at the output of the low-pass filter section being used. From the output of the low-pass filter, A2A1-E8, the signal is applied to T/R relay K1, pins 3 and 5. The relay, deenergized in receive, routes the signal out of A2A2 at P1. From P1 the received signal is routed to A9J4, the rear panel antenna relay jack. With a single antenna, A9J4 is jumpered to A9J8, RCV IN, filtered by TB1 and applied to A3 at J9.

With separate receive and transmit antennas, the receive antenna is connected directly to J8, RCV IN, and the jumper between A9J4 and A9J8 is removed. The receive signal from the antenna is filtered by TB1, L-C filter, and applied to A3 at J9 without being routed through the T/R relay.

3.3.2 Receive-Exciter A3

This section covers the receive circuits from the rf input on A3 to the input of the noise blanker A11. To follow the signal path, refer to receiver-exciter block diagram figure 3.3 and the schematic diagrams in the service manual, beginning on sheet 1 of 8.

The receive signal enters the receiver/exciter circuits at A3J9, sheet 1 of the receiver-exciter schematic. L800-L804, C800, C801, R800, and R801 form a 1.6-MHz high-pass filter which provides broadcast band desensitization by attenuating frequencies in the 0.5- to 1.6 MHz range. From the output of the high-pass filter, the signal is coupled through C802 to the switchable high-pass filters. The receive signal is applied to four diode switches, CR800, CR802, CR804, and CR806 simultaneously; however, only one diode is forward biased at a time. The four diode switches all have +9 V dc applied to their anodes in receive operation by the +9 V dc RCV through R802 and L818. One of these diodes will have a ground applied to its cathode from Q906, Q907, Q908, or Q909 on schematic sheet 7. There are also four diode switches at the outputs of the filters, each with +9 V dc applied to its cathode and the switching action again controlled by the inputs from sheet 7. The receive operating frequency determines which filter section will be enabled.

From the high-pass filter, the signal is applied to a peak-to-peak limiter circuit comprises of CR100, CR101, VR100, C100, and C101. If the incoming receive signal exceeds + or -6.8 V the zener diodes will conduct, limiting the signals peak-to-peak amplitude to approximately 13.6 volts.

From the limiter, the signal is applied to diode switches CR103 and CR107. During receive operation CR103 and CR107 are forward biased by +9 V dc applied to their anodes through L141 and L102. C104 and pin diode CR104 at the junction of CR103 and CR107 are part of the automatic gain control (AGC) circuit. The voltage of AGC 3, from the emitter of Q403 controls the conduction of pin diode CR104. With a weak received signal, CR104 is reversed biased and no attenuation takes place. With large signals, the pin diode is forward biased and some signal is shunted to ground through C104 and CR104. See figure 9-11.1 for pin diode characteristics. Diode switch CR108 is reversed biased during receive operation.

From CR107 the receive signal path is through a low-pass filter comprised of C106-C114 and inductors L105-107. The filter, a 30-MHz low-pass, passes signals within the operating range of the KWM-380, 0.5 to 29.99999 MHz, with little attenuation. Incoming signals above 30 MHz are attenuated signficantly by the filter. The 30-MHz low-pass filter also prevents unwanted signals present at U100, pin 1 from feeding back to the receive input circuits.

From the filter, the receive signal is applied to mixer U100 pin 1. The second input to double-balanced mixer U100 is the variable injection from the synthesizer A5A1P1. This injection ranges from 39.645 MHz with a dial frequency of 00.50000 to 69.14999 MHz with a dial frequency of 29.99999. The injection can vary in 10-Hz steps and is automatically selected with the front panel frequency control. The injection to pin 8 of U100 is approximately +17 dBmW and is always 39.145 MHz above the desired receiver signal, to develop the 39.145-MHz first receive if.

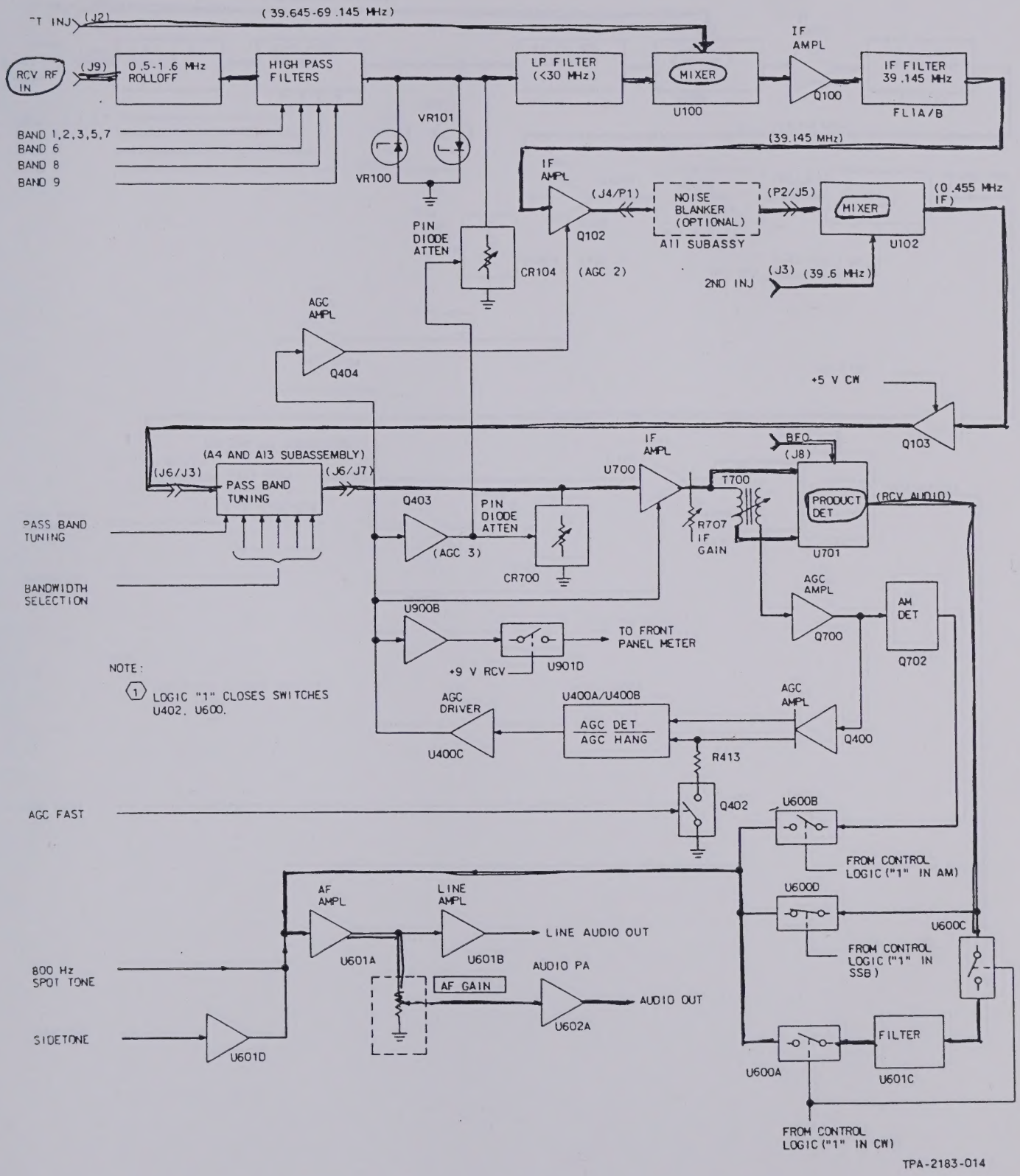


Figure 3-3. Receive Signal Path Block Diagram.

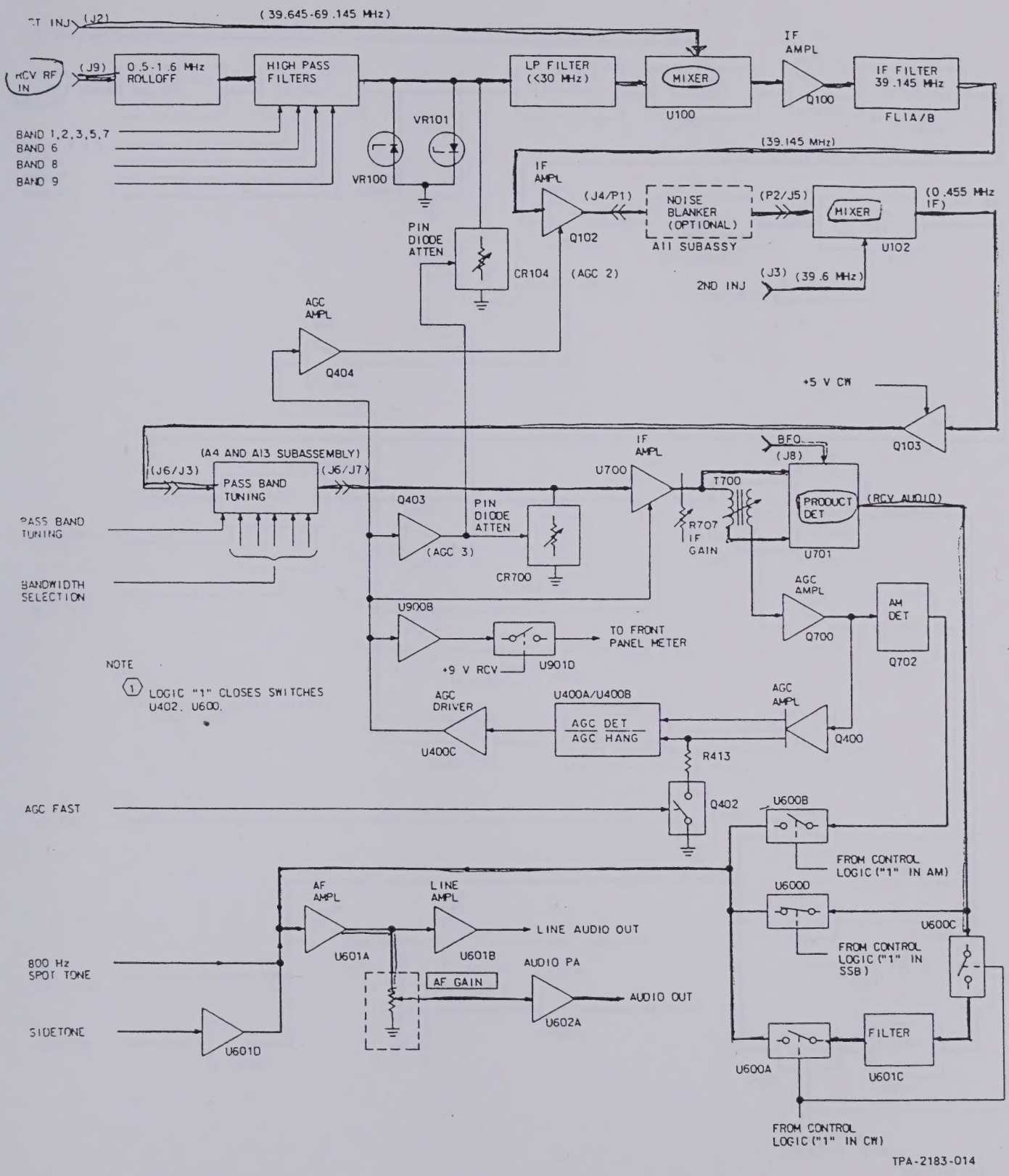


Figure 3-3. Receive Signal Path Block Diagram.

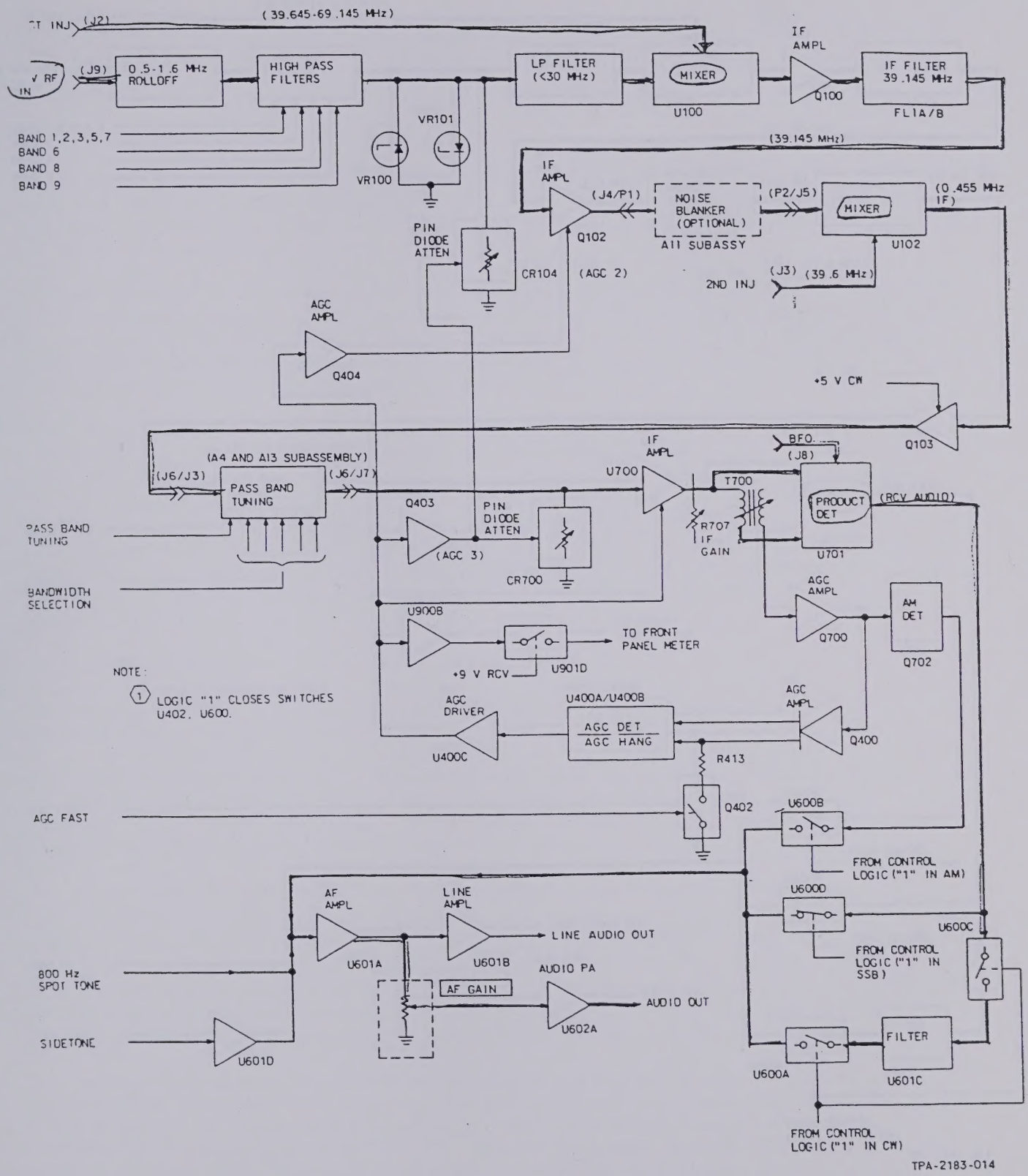


Figure 3-3. Receive Signal Path Block Diagram.

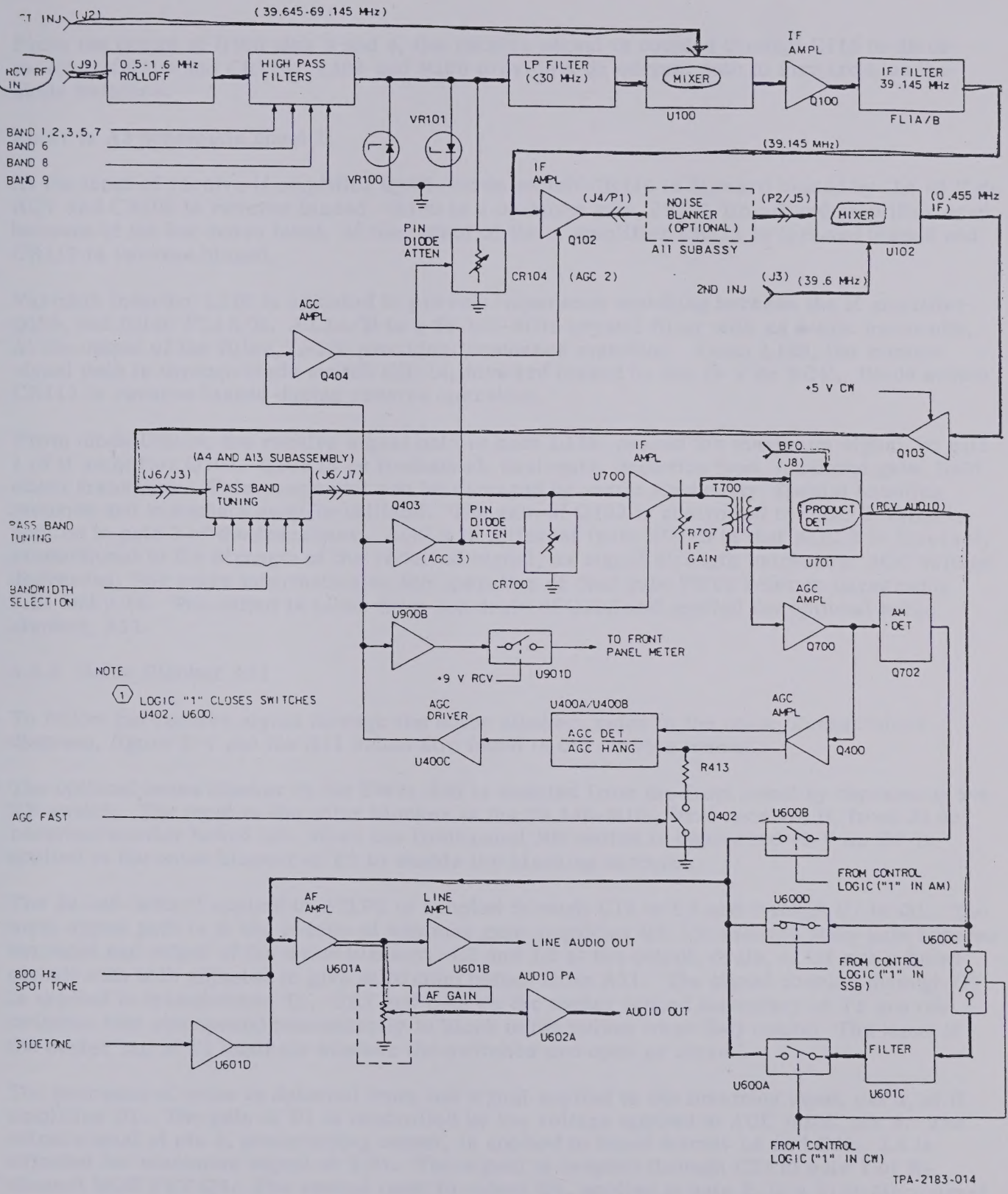


Figure 3-3. Receive Signal Path Block Diagram.

From the output of U100 pins 3 and 4, the receive signal is coupled through C115 to diode switches CR109 and CR110. L108 and R106 provide a dc current path to forward bias the diode switches.

Refer to A3 schematic sheet 2.

At the input of receive if amplifier Q100, diode switch CR110 is forward biased by the +9 V dc RCV and CR109 is reverse biased. Q100 is a common gate, JFET, broadband amplifier used because of its low-noise level. At the output of the if amplifier CR111 is forward biased and CR112 is reverse biased.

Variable inductor L119 is adjusted to provide impedance matching between the if amplifier Q100, and filter FL1A/B. FL1A/B is a 39.145-MHz crystal filter with an 8-kHz bandwidth. At the output of the filter, L-120 provides impedance matching. From L120, the receive signal path is through diode switch CR114, forward biased by the +9 V dc RCV. Diode switch CR113 is reverse biased during receive operation.

From diode CR114, the receive signal path is past L123, peaked for maximum signal, to gate 1 of if amplifier Q102. Q102 is an N-channel, dual-gate, depletion type, insulated gate, field effect transistor. This component can be damaged by static electricity. Special handling methods and materials must be utilized. The gain of Q102 is controlled by AGC 2 which is applied to gate 2 of the transistor. AGC 2 is different from AGC 3 in that AGC 2 is inversely proportional to the strength of the received signal, as signal strength increases, AGC voltage decreases. For more information on the operation of dual gate FETs refer to paragraphs 9.14 and 9.15. The output is taken from the drain of Q102 and applied the optional noise blanker, A11.

3.3.3 Noise Blanker A11

To follow the receive signal through the noise blanker, refer to the noise blanker block diagram, figure 3-4 and the A11 schematic found in the service manual.

The optional noise blanker in the KWM-380 is enabled from the front panel by depressing the NB switch. The input to the noise blanker is the 39.145-MHz, first receive, if, from J4 on receiver/exciter board A3. When the front panel NB switch is depressed +9 V dc SW is applied to the noise blanker at E2 to enable the blanking circuits.

The 39.145-MHz if applied to A11P1 is coupled through C16 to U1 and through C1 to Q1. The main signal path is to the source of common gate amplifier Q1. Q1 assures unity gain between the input and output of the noise blanker. L1 and L2 at the output, drain, of Q1 are a tuned circuit with both adjusted to give maximum output from A11. The signal coupled through C6 is applied to transformer T1. CR1 and CR2 on the center tapped secondary of T1 are the switches that are opened momentarily to block noise pulses when they occur. The input at the center tap of T1 controls whether the switches are open or closed.

The presence of noise is detected from the signal applied to the inverting input, pin 4, of if amplifier U1. The gain of U1 is controlled by the voltage applied to AGC input, pin 5. The output signal at pin 8, noninverting output, is applied to tuned circuit L4 and C20. L4 is adjusted for maximum signal at TP3. The signal is coupled through C21 to gate 1 of N-channel MOS FET Q4. The second input to mixer Q4, applied to gate 2, is a 31.0-MHz signal from crystal controlled oscillator Q3. The output of the oscillator, measured with a high-impedance rms voltmeter between TP5 and the ground side of R13, must be 0.75 V rms or greater. The 39.145-MHz and 31.0-MHz signals are mixed at Q4 to produce an 8.145-MHz signal.

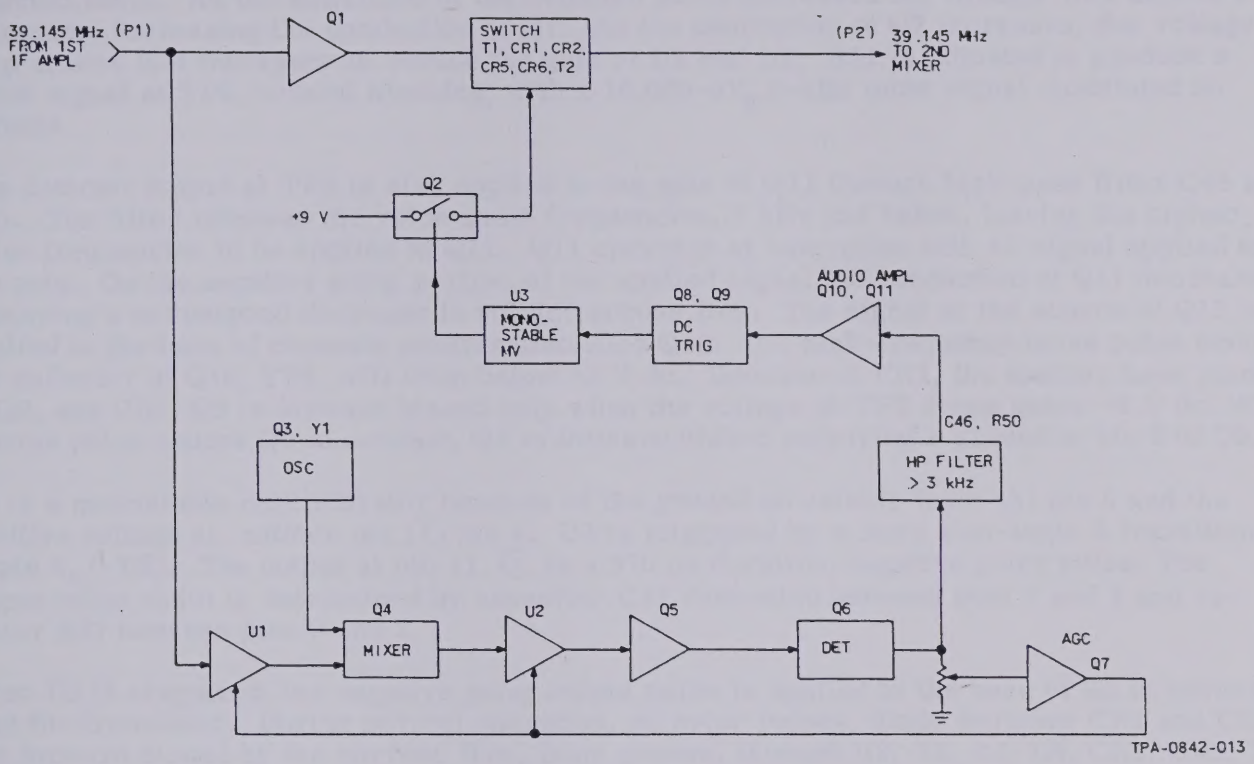


Figure 3-4. Noise Blanker Block Diagram.

The output, at the drain of Q4, is applied to tuned circuit L5 and C26. L5 is adjusted to couple the maximum 8.145 MHz to if amplifier U2 through C25 and R51. Pin 4 is the inverting input of U2 and pin 6 is the noninverting input. The gain of U2 is controlled by the AGC voltage applied at pin 7. As the input signal to A8 increases the AGC voltage increases to reduce the gain of U2, keeping the output of U2 at a constant level. The output, at noninverting output, pin 8, is applied to tuned circuit L7 and C32. L7 is adjusted to couple maximum 8.145 MHz through C33 to gate 1 of Q5. Q5 is an N-channel MOS FET with a constant gain determined by the +3.5 V dc at gate 2. The output, at the drain of Q5, is peaked by L8, in tuned circuit L8 and C37, before it is applied to the gate of detector Q6.

Q6 is an N-channel, depletion mode, field effect transistor that is biased to saturation with no signal applied. With a modulated signal applied to the base, the conduction of Q6 is reduced below saturation during the negative half of the modulation envelope. As the bias of Q6 is reduced below saturation the conduction of Q6 decreases giving a corresponding decrease in voltage at the source. C41 removes the 8.145-MHz component from the output of the detector leaving the demodulated audio at TP3.

The output at TP3 is used to develop the AGC voltage that controls the gain of U1 and U2. With no output from the detector, the conduction of Q7 is determined by the setting of variable resistor R31 and fixed resistors R32 and R33. At this time the voltage drop across R32, TP4 is low enough to keep the gain of U1 and U2 at maximum. With output from the detector, at TP3 the negative swing of the audio reduced the voltage drop across R31 and R32.

Capacitor C42 filters the audio to produce a dc voltage equal to the average amplitude of the detected audio. As the amplitude of the detected audio increases the voltage drop across R33 increases, increasing the conduction of Q7. As the conduction of Q7 increases, the voltage drop across R34 increases to reduce the gain of U1 and U2. R31 is adjusted to produce a 2.0-V signal at TP2, without blanking, with a 10,000-μV, 5-kHz input signal modulated 90 percent.

The detector output at TP3 is also applied to the gate of Q11 through high-pass filter C46 and R50. The filter removes the voice audio frequencies, 3 kHz and below, leaving the higher noise frequencies to be applied to Q11. Q11 operates at saturation with no signal applied to the gate. On the negative going portion of the applied signal the conduction of Q11 decreases producing a correspond decrease in voltage across R49. The signal at the source of Q11 is applied to the base of common emitter amplifier Q10. If a high-frequency noise pulse occurs, the collector of Q10, TP2, will drop below +2 V dc. Because of VR1, the emitter base junction of Q9, and CR3, Q9 is forward biased only when the voltage at TP2 drops below +2 V dc. When a noise pulse causes Q9 to conduct, Q8 is forward biased supplying a ground to pin 6 of U3.

U3 is a monostable multivibrator because of the ground on astable input (A) pin 5 and the positive voltage at astable not ($\overline{A}$) pin 4. U3 is triggered by a logic 1-to-logic 0 transition at pin 6, (-TR). The output at pin 11, $\overline{Q}$, is a 370 μs duration, negative going pulse. The output pulse width is determined by capacitor C47 connected between pins 3 and 1 and resistor R37 between pins 3 and 2.

When U3 is triggered, the negative going output pulse is applied to the base of Q2 to reverse bias the transistor. During normal operation, no noise pulses, diode switches CR1 and CR2 are forward biased by the current flow, from ground, through R8, T2, R5, R6, CR1, CR2, T1, Q2 and R10 to the +9 V dc supply. With CR1 and CR2 forward biased, the 39.145-MHz receive if is passed to the blanker output P2. When a noise pulse is received and detected, Q2 turns off, reverse biasing the diodes to block the noise pulse from the output P2. The effeciency of the noise blanker circuit is improved by the effect of crystal filter FL1A/B on the receiver/exciter board A3. Short duration noise pulses are stretched by the filter to approximately 150 microseconds. As the stretched pulse starts through the diode switch it is also being routed to the other parts of the noise blanker. Before the noise pulse can build in amplitude to a level to be heard above the normal audio output it has been detected and the multivibrator output developed to reverse bias the diode switches. Reverse biasing the diodes for 370 microseconds gives the pulse time to rise and decay before the diodes are turned back on to pass the signal. The 370 microsecond absence of the signal is not detectable to the listener in hearing the normal audio output of the receiver.

When the noise blanker is turned off, front panel NB switch not depressed, the +9 V dc SW voltage is removed from A11 E2, disabling the noise detector. With the noise detector circuits disabled, diodes CR1 and CR2 remain on regardless of the noise pulses on the receive if signal. If the optional noise blanker is not installed, the signal at A3J4 is routed directly to A3J5.

3.3.4 Second Receive Mixer

Refer to figure 3-3 in the self-study manual and the A3 schematic, sheet 3, in the KWM-380 Service Manual.

The output of the noise blanker re-enters A3 at J5. The output of the optional noise blanker, 39.145 MHz, is input to double balanced mixer, U101 at pin 1. The second input to the mixer, 39.600 MHz, from the frequency standard, is applied to pin 7 through diode switch CR117.

CR117 is forward biased during receive operation by current flow from ground through R124, L131, CR117, and L130 to the +9 V dc RCV. The mixer output, the 445-kHz, second receive , at pins 3 and 4 is coupled through C179 and C147 to the base of amplifier Q103. The gain of Q103 is determined by the mode of operation, in AM or SSB, R120 is unbypassed producing degeneration to lower the gain. In CW operation the +5 V dc CW from Q917, sheet 6, is applied through R145 and L145 to the anode of CR124. This forward biases CR124 and C180 is added to the circuit as a bypass for R120. With R120 bypassed, the gain of Q103 is increased by approximately 6 dB. From the collector of Q103, the receive signal is applied to diode switch CR115. CR115 is forward biased during receive operation by current flow from ground through R123, CR115, and L129 to the +9 V dc RCV. During receive operation CR116 is reverse biased and the receive signal is coupled through C152 to A3J6 where it enters the variable if (passband tuning circuit).

3.3.5 Passband Tuning Circuit A4

Refer to figures 3-5, 3-6, and 3-7 in the self-study manual and the passband tuning circuit schematic A4 in the service manual. The passband tuning circuit determines whether the detected receive signal will be upper-side band, lower-sideband or AM.

The passband tuning circuit also provides a means of eliminating adjacent channel interference by varying the if frequency as it passes through one of the passband tuning circuit bandpass filters.

The 455-kHz output of the second receiver mixer enters the passband tuning circuit at J9, and is applied to the input of double-balanced mixer U4, through low-pass filter L1, C1, and C2. The second input to mixer U4, applied to pin 8, is a variable 6.71 MHz from injection oscillator Q2.

The operating frequency of the injection oscillator is controlled by the 6.71-MHz crystal Y1 and the dc voltage applied to voltage variable capacitor CR13. By varying the positive dc voltage applied to the cathode of CR13, the capacitance of CR13 and the oscillators operating frequency can be changed. C16 is a fine frequency adjust for the oscillator.

The amount of reverse bias voltage applied to CR13 is dependent on the setting of the selectivity control (PBT) on the front panel. When the KWM-380 is operating in the receive mode, pin 16 of J1 will have a logic 1 present while pins 10, 12, and 14 are at logic 0. The logic 1 at pin 16, applied to U3D, pin 11, will cause the output of U3D to go to +18 V. This is applied to pin 12 of U1D to close the switch. With U1D closed, the voltage from the variable resistor front panel PBT knob, is applied through R56 and R40 to CR13.

Because the setting of the front panel PBT control controls the oscillator frequency during receive operation it also controls which sideband (if any) will be removed. For AM reception, the oscillator is adjusted to 6.71 MHz so that when it is mixed with the incoming 455 kHz the result is a 6.255-MHz signal which is equal to the center frequency of the passband filters. For lower sideband reception the oscillator frequency is increased above 6.71 MHz which increases the mixer output above 6.255 MHz. By doing this, the center frequency and the upper sideband fall outside of the filters passband while the lower sideband falls within the passband. This removes the carrier and upper sideband, leaving the lower sideband to be detected. To receive an upper sideband signal the oscillator frequency is decreased to move the carrier and lower sideband below the passband of the filter.

The signal path from the oscillator to the mixer is from the collector of Q2 to Q3, from the collector of Q3 to Q4 and from the emitter of Q5 through R1 and C9 to mixer U4.

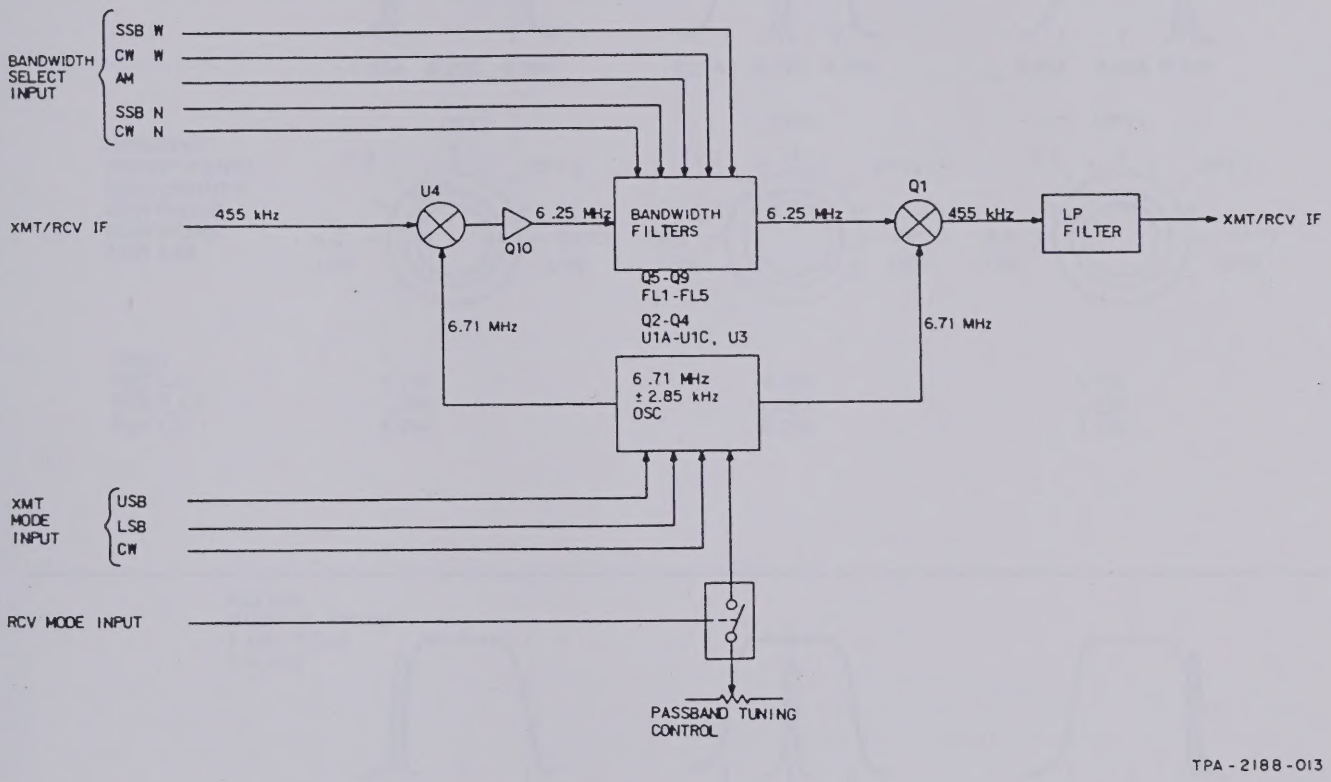
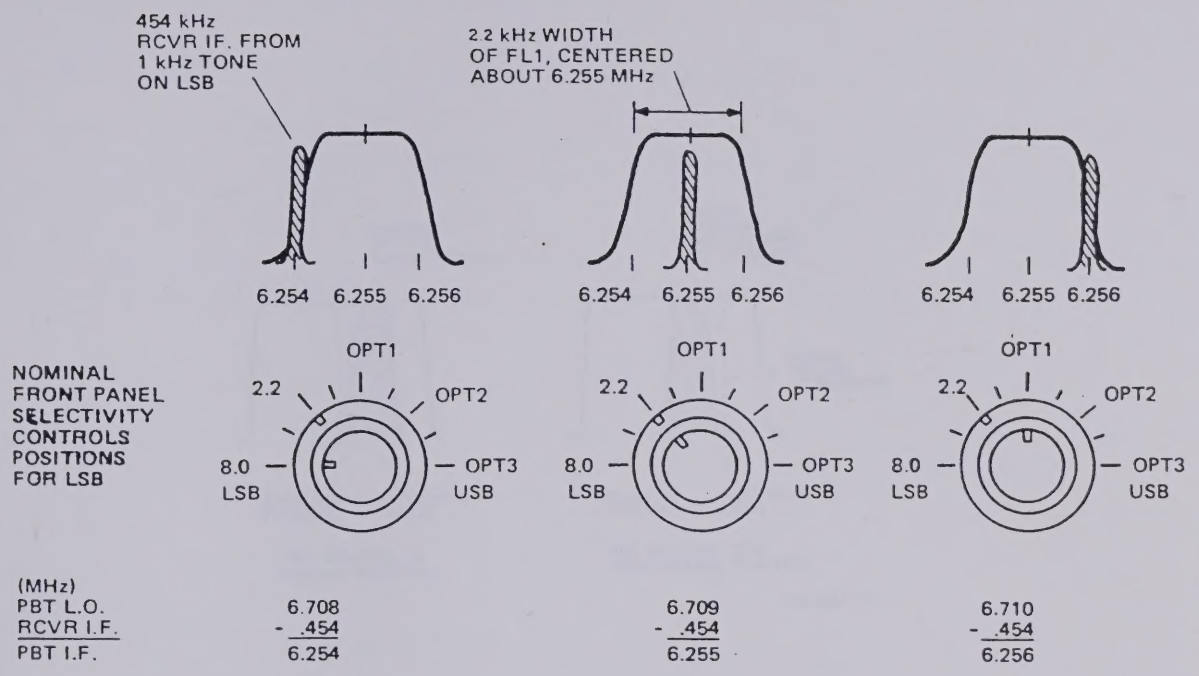


Figure 3-5. Passband Tuning Block Diagram.



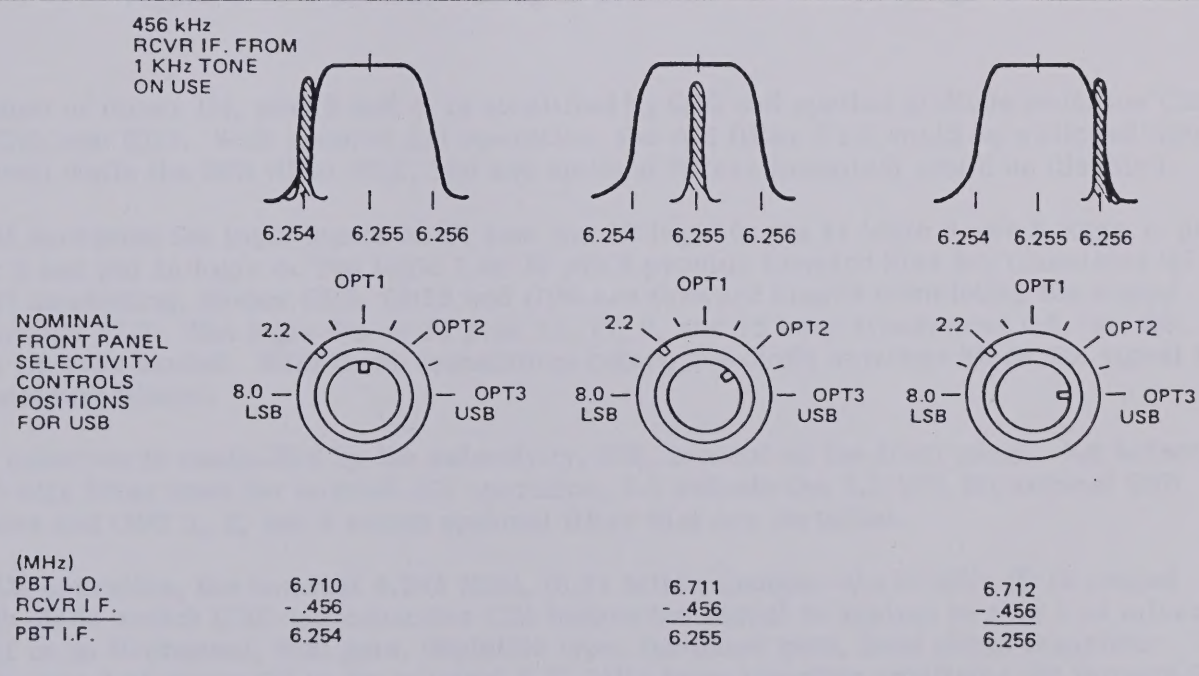


Figure 3-6. Front Panel Selectivity Controls.

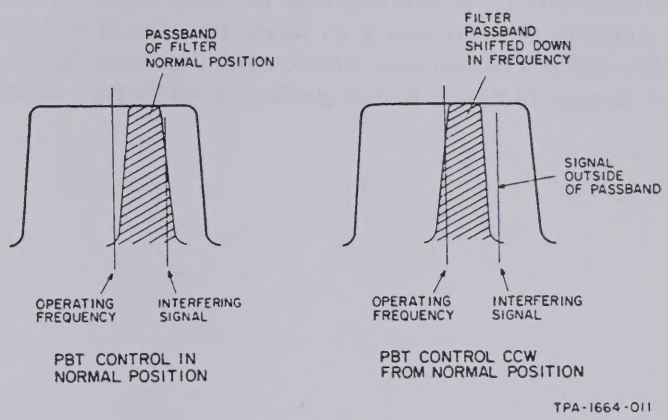


Figure 3-7. Passband Tuning to Eliminate Interferring Signal.

The output of mixer U4, pins 3 and 4, is amplified by Q10 and applied to diode switches CR1, CR3, CR5, and CR9. With receive AM operation, the AM filter FL3 would be switched into the circuit while the SSB filter FL1, and any optional filters installed, would be disabled.

For AM operation the logic inputs on J1 are: pin 13 logic 0, pin 11 logic 0, pin 8 logic 1, pin 9 logic 0 and pin 15 logic 0. The logic 1 on J1 pin 8 provide forward bias for transistor Q7. With Q7 conducting, diodes CR5, CR18 and CR6 are forward biased completing the signal path through FL3. The logic 0's on J1 pins 13, 11, 9, and 15 keep transistors Q5, Q6, Q8, and Q9 reverse biased. With these transistors cutoff, the diode switches block the signal from the remaining filters.

Filter selection is controlled by the selectivity, BW, control on the front panel. 8.0 selects the 8.0-kHz filter used for normal AM operation, 2.2 selects the 2.2-kHz for normal SSB operation and OPT 1, 2, and 3 select optional filter that are installed.

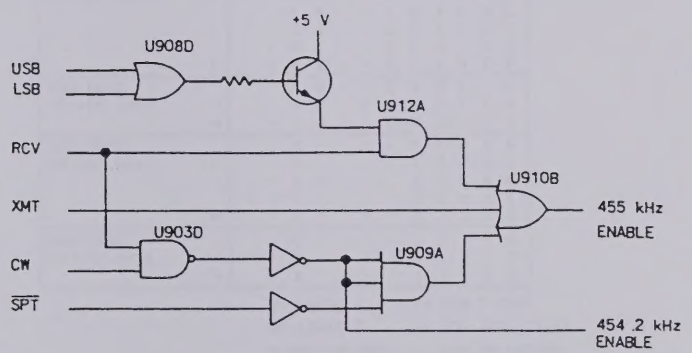
With AM operation, the nominal 6.255 MHz, (6.71 MHz injection -0.455 MHz if) is routed through diode switch CR6 and capacitor C24 before the signal is applied to gate 1 of mixer Q1. Q1 is an N-channel, dual gate, depletion type, insulated gate, field effect transistor. The input to gate 2 of mixer Q1 is the nominal 6.71 MHz from injection oscillator Q2 through Q3. The output of the mixer at the drain of Q1 is filtered by the low-pass filter consisting of C29, C30, C40, C41, C53, L6, L16, L17, and L18 to give a nominal 455 kHz signal at the output of the passband tuning circuit J6.

Integrated circuit regulator U2 provides a regulated +18 V dc from the +24 V dc regulated input at J1 pin 3, for use in the passband tuning circuit.

3.3.6 IF Amplifiers, Detectors and Audio Output A3

Refer to block diagrams, figures 3-1, 3-8, and 3-9 and A3 schematic sheet 3.

The 455-kHz if re-enters the receiver/exciter circuits at A3J7. The signal is blocked by reverse biased CR119 and passes through forward biased diode CR120. At the junction of C701 and C702 the AGC voltage, AGC 3, and pin diode CR700 control the amplitude of the if signal. AGC 3, from the collector of Q403 is a positive dc voltage proportional to received signal strength. As signal strength increases, pin diode CR700 will be forward biased to maintain a constant audio output by shunting some of the if signal to ground.



		USB	LSB	CW	AM	SPT	KI	TXI	PTT	TUNE	LOL	TF	KEY	XMT	RCV
455 kHz ENABLE	=0	0	0	0	-	X	-	-	-	-	-	-	-	0	X
		X	X	X	-	1	-	-	-	-	-	-	-	0	0
455 kHz ENABLE	=1	X	X	X	-	X	-	-	-	-	-	-	-	1	X
		1	X	X	-	X	-	-	-	-	-	-	-	X	1
		X	1	X	-	X	-	-	-	-	-	-	-	X	1
		X	X	1	-	0	-	-	-	-	-	-	-	X	1
454.2 kHz ENABLE	=1	-	-	1	-	-	-	-	-	-	-	-	-	-	1
	=0	-	-	1	-	-	-	-	-	-	-	-	-	-	0
	=0	-	-	0	-	-	-	-	-	-	-	-	-	-	1

1= LOGIC 1 X= DON'T CARE
0= LOGIC 0 -= NOT APPLICABLE

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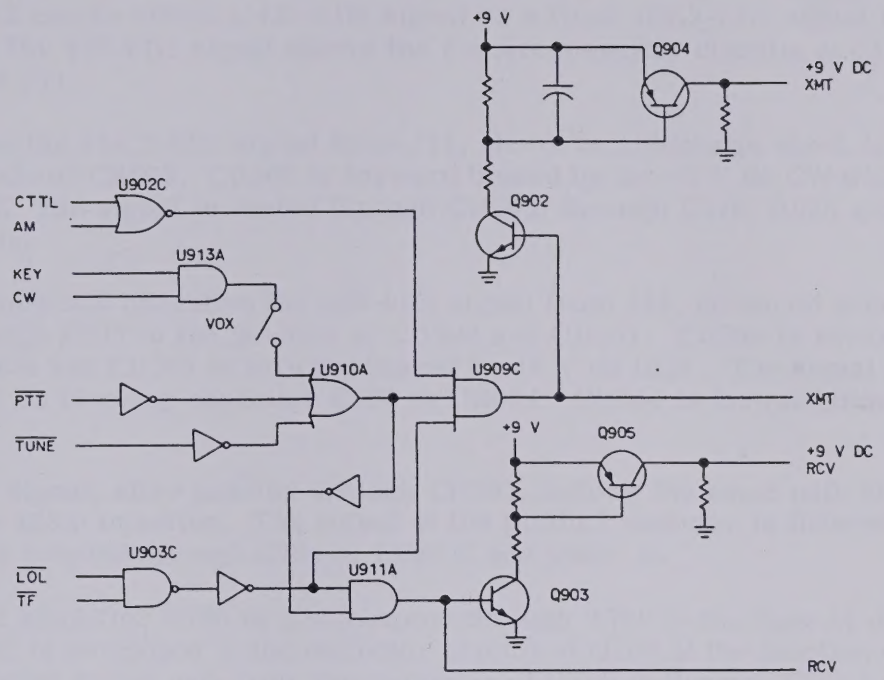
Figure 3-8. BFO Enable Simplified Logic Diagram and Chart.



	USB	LSB	CW	AM	SPT	KI	CTTL	PTT	TUNE	LOL	TF	KEY
XMT (AND +9 V DC XMT) =0	-	-	X	X	-	-	1	X	X	X	X	X
	-	-	X	1	-	-	X	X	X	X	X	X
	-	-	X	X	-	-	X	X	X	0	X	X
	-	-	X	X	-	-	X	X	X	X	0	X
	-	-	0	X	-	-	X	1	1	X	X	X
	-	-	X	X	-	-	X	1	1	X	X	0
*	-	-	X	X	-	-	X	1	1	X	X	X
XMT (AND +9 V DC XMT) =1	-	-	X	0	-	-	0	X	0	1	1	X
	-	-	X	0	-	-	0	0	X	1	1	X
**	-	-	1	0	-	-	0	X	X	1	1	1
RCV (AND +9 V DC RCV) =0	-	-	X	-	-	-	-	X	X	0	X	X
	-	-	X	-	-	-	-	X	X	X	0	X
	-	-	X	-	-	-	-	X	0	X	X	X
	-	-	X	-	-	-	-	0	X	X	X	X
**	-	-	1	-	-	-	-	X	X	X	X	1
RCV (AND +9 V DC RCV) =1	-	-	0	-	-	-	-	1	1	1	1	X
	-	-	X	-	-	-	-	1	1	1	1	0
*	-	-	X	-	-	-	-	1	1	1	1	X

1= LOGIC 1 X= DON'T CARE
0= LOGIC 0 -= NOT APPLICABLE
* VOX SW OPEN ** VOX SW CLOSED

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Figure 3-9. +9 V dc XMT and RCV Simplified Logic Diagram and Chart.

Variable resistor R702 adjusts the receive if gain. U700 is a two-stage if amplifier, pin 14 is the inverting input, pin 1 is the noninverting input and pin 12 is the output of the first stage. The output at pin 12 is coupled through C705 to the input of the second stage, pin 10. Pin 7 is the noninverting output of the second stage and pin 8 is the inverting output. AGC 1, a dc voltage proportional to signal strength is applied to U700 pins 3 and 4 to control the gain of the amplifier. During transmit operation the +9 V dc XMT through CR701 and R706 reduce the gain of U700 to minimum. Variable resistor R707 at the output of U700 is an if gain adjustment.

The 455-kHz output of if amplifier U700 is applied to the inputs of product detector U701 pins 1 and 5. The second input to the product detector is applied at pin 2 through C716. The signal entering at pin 2 can be either a 455-kHz signal or a fixed 454.2-kHz signal from oscillator assembly A7. The 455-kHz signal enters the receiver/exciter circuits at J10, the 454.2-kHz signal enters at J11.

In CW operation the 454.2-kHz signal from J11, shown on schematic sheet 4, is coupled through C520 to the anode of CR505. CR505 is forward biased by the +5 V dc CW while CR504 is reverse biased. The signal is routed through CR505, through C519, R526 and C716 to the product detector.

During single sideband operation the 455-kHz signal from J10, shown on schematic sheet 4, is coupled through C517 to the junction of CR500 and CR501. CR500 is reverse biased during receive operation and CR501 is forward biased by +9 V dc RCV. The signal passes through CR501, through dc blocking capacitor C523 to CR504. CR504 is forward biased by the +5 V dc SSB.

The 454.2-kHz signal, after passing through CR505, follows the same path to the product detector as the 455.0 injection. The output of the product detector is filtered by C718, C719, and R715 and is coupled through C720 to U600 C and U600 D.

The output of if amplifier U700 is also coupled through T700 to the base of AGC amplifier Q700. The AGC is developed in the collector circuit of Q700 at the junction of R720 and R721. The receive signal path from the collector of Q700 is through C725 to the base of AM detector Q702. Q701 provides the temperature compensated operating point of AM detector Q702. The amplitude modulated signal applied to the base of Q702 will cause the conduction to vary at the rate of the modulating signal. The detected signal at the emitter of Q702 is filtered by the low pass filter C726, C727, R723, and R724. After being filtered, the audio signal is coupled through C728 to switch U600B.

Refer to schematic sheet 5.

In single sideband operation switch U600D is enabled by a logic 1 on pin 12 from the emitter of Q915. With this switch enabled the detected audio is applied to the noninverting input of U601A.

During CW operation, switches U600C and U600A are enabled by a logic 1 on pins 6 and 13, from J12 pin 8. With these switches enabled the CW output of the product detector is routed to U601C. U601C is an 800-Hz active audio filter that amplifies the detected CW audio before it is applied to U601A.

In AM operation a logic 1 from J12 pin 9 is applied to pin 5 of U600B to enable the switch. With the switch enabled audio from the AM detector is routed to the noninverting input of U601A.

When the SPOT button on the front panel is depressed, while operating in CW receive, the control logic enables the 455-kHz at J10 and the 454.2-kHz at J11. The 455-kHz signal at J10 is routed through CR501 to the gate of Q501. The 454.2-kHz signal at J11 is coupled through C502 and C524 to the gate of Q502. The two signals are amplified by Q501 and Q502 and combined at the junction of R534, R535, CR506, and CR507 to produce an 800-Hz signal that is routed to low-pass filter L600, C611, and C612. At the output of the low-pass filter, variable resistor R615 adjusts the level of 800-Hz signal applied to the inverting input of U601A. By varying the receive dial frequency until the received CW tone is equal to the injected 800-Hz, the frequency of a transmitted signal can be spotted.

If a loss-of-lock (LOL) occurs in the synthesizer a logic 0 is applied to receiver-exciter A3J13 pin 6, $\overline{\text{LOL}}$, shown on schematic sheet 6. If a tune fault occurs in the pa/coupler filter assembly, a logic 0 is applied to the receiver-exciter at J20 pin 2, $\overline{\text{TF}}$. This circuit is not currently used but may be in the future with a coupler or external pa. Either of these inputs at logic 0 will produce a logic 1 at U903C, pin 10, which is applied to pin 5 of NAND gate U903B. U903B, U905A, C900, and R920 make up a 5-Hz generator that is enabled by a logic 1 at U903B pin 5. The output of the 5-Hz generator is applied to OR gate U908A pin 1. With pin 2 of U908A at logic 0, the output of the 5-Hz generator is enabled through U908A to enable the 1-kHz generator, U903A, U905G, C901, and R921. Pin 2 of U908A is a logic 0 with J20 pin 3, $\overline{\text{KI}}$ at "0", J16 pin 15, $\overline{\text{KEY}}$ at "0", J12 pin 8, CW at "1" , J20 pin 1, $\overline{\text{TUNE}}$ at "1" and transmit operation. The output of the 1000-Hz generator is applied through level adjustment R616 to the inverting input of operational amplifier U601D, shown on sheet 5. The noninverting input of U601D has approximately +6.5-V dc offset voltage applied to it. U601D is used as a square wave-to-sine wave converter. The output of U601D, pin 14 is applied to the inverting input of audio amplifier U601A and to the VOX circuit through C550, R551, and C504 on receiver-exciter schematic sheet 4.

U601 is a high-gain audio amplifier, voltage gain of approximately 30, with a nearly flat frequency response throughout the 300-to 2400-Hz audio frequency range. The audio input to U601A can be on either the inverting or noninverting inputs, depending on the signal source. The output of U601A, pin 1, is coupled through C614 to the VOX circuit, AF GAIN pot R622, and U601B, through C615. The signal supplied to the VOX circuit is the anti-VOX audio input. The audio coupled through C615 is applied to the noninverting input, pin 5, of U601B. U601B, with a nearly flat frequency response, amplifies the audio signal to produce a -10-dB mW output at J6, AUD OUT on the rear panel of the KWM-380.

Variable resistor R622 is a front panel control, AF GAIN (small knob) and is used to control the audio output level at the front panel PHONES jack, internal speaker, and rear panel, external speaker jack, SPKR, J11. The audio from R622, J32, is coupled through C620 to audio amplifier U602A, noninverting input, pin 1. The frequency response of U602A is nearly flat with a slight roll-off in gain at the high end of the audio output range. The audio out of U602A, pin 4, is coupled through C624 to the internal speaker, front panel phones jack and rear panel external speaker jack. With the receiver gain at maximum the audio output is 3.5 watts or greater into a 4-ohm load. The total harmonic distortion in the audio output is not more than 10 percent with a 1-kHz signal. The audio output frequency response is not more than 5 dB of variation from 300 to 2400 Hz.

Connecting phones to the front panel PHONES jack inhibits the internal speaker and the rear panel speaker (SPKR) outputs. Connecting an external speaker to the rear panel SPKR jack inhibits the internal speaker and the PHONES jack.

3.3.7 Receive AGC Circuits and Switching Circuits

Refer to block diagram figure 3.1 and A3 schematic, sheets 1 and 3.

The purpose of the AGC circuits is to automatically adjust the gain of the receive circuits so that the audio output level remains constant with changes in received signal strength. This is accomplished by monitoring the signal amplitude at the input of the detector. With no signal or a very small received signal (2 μV rf input), the receiver gain is at maximum. As received signal strength increases above 2 μV, the increase is detected and the receiver gain is reduced to keep the audio output constant. The AGC limits the audio output to not more than 8 dB of variation for open circuit rf input variations from 2-μV- to 100-mV.

Refer to schematic diagram, sheet 1.

The AGC circuit has three inputs, the if sample from the collector of AGC amplifier Q700, +5 V dc AGC off at J12 pin 15 and +5 V dc AGC fast at J12 pin 16. The if AGC signal is plied to the base of common emitter amplifier Q400 and from the collector of Q400 through R403 to the collector of Q401. Q401 is a transistor switch used to enable or disable the AGC. With +5 V dc at J12 pin 15, Q401 is forward biased, grounding the if AGC signal at its collector. With a logic 0 at J12 pin 15, Q401 is cutoff, allowing the if AGC signal to be coupled through C402 to diodes CR400 and CR401. The setting of variable resistor R409, rf gain, determines the voltage on the anode of CR401, which will affect the level of dc voltage on C406 from the if AGC sample rectified by CR400. The dc voltage on C406 is applied to the noninverting input of U400A. When the output of U400A pin 1 reaches a positive dc voltage sufficient to forward bias CR404, current flow through R409 will produce a dc voltage which is applied to the noninverting input of U400C. U400C, with 100 percent negative feedback is a unity gain amplifier. As the dc voltage of the input of U400C pin 10 increases, there will be a corresponding increase at the output, pin 8. When the output voltage of U400C exceeds +3.6 V, current will flow through VR400, forward biasing transistor Q403 and Q404 to develop AGC 2 and 3 and develop AGC 1 voltage across resistors R425 and R426.

With emitter follower Q403 forward biased, a current path is provided to forward bias pin diode CR104 in the rf section and pin diode CR700 in the if section. If the AGC 3 voltage at the emitter of Q403 is monitored, it should increase as the strength of the received signal increases, and vice versa. If the AGC 3 voltage is monitored with constant amplitude rf input signal, adjusting the front panel rf gain control towards minimum gain will increase the voltage and adjusting the rf gain towards maximum will decrease the AGC 3 voltage. The AGC 1 voltage, will change in the same manner as the AGC 3 voltage with changes in received signal strength and rf gain control settings.

AGC 2 voltage is inversely proportional to received signal strength because of the inversion that occurs in common emitter transistor Q404. As signal strength increases or as the rf gain is adjusted towards minimum the AGC 2 voltage, applied to gate 2 of receive if amplifier Q102, will decrease.

The if AGC sample at the collector of Q400 is coupled to diodes CR402 and CR403 through C404. With the rf gain control determining the minimum reference, the AGC sample is rectified at CR403 to produce a dc voltage on C405 proportional to the signal strength. With the front panel AGC control set for slow, J12 pin 16 at logic 0, transistor Q402 is reversed biased removing R413 from the circuit. With R413 out of the circuit C405 and C407 have a slow discharge path through 2.2 megohm resistor R416. This slow discharge time increases the time required for the output of U400B to decrease to the point where CR405 is forward biased.

With +5 V dc present at J12 pin 16, transistor Q402 is forward biased and resistor R413, 560-kΩ, is placed in the circuit. With R413 in the circuit the discharge time of C405 and C407 is reduced. This decreases the time required for the output of U400B to decrease after a loss or reduction of amplitude in the received signal. When the output of U400B decreases sufficiently to forward bias CR405, the dc voltage input to U400C pin 10, is reduced to increase the gain of the receiver. The slower AGC release time (switch depressed) is normally used for SSB reception while the fast AGC action is used withCW.

The switching circuits that control the receive and transmit circuits on the receive-exciter board are shown on the A3 schematic, sheets 6 and 7. Although the switching affects both the receive and transmit operation it will only be explained in the receive signal flow section.

This explanation will begin ay analyzing the inputs to the circuits shown on schematic sheet 6 and figures 3-8 and 3-9. USB input at J12 pin 10 is an input from the front panel mode switch,

S4. When USB operation is selected, +5 V dc is applied to pin 10 from the switch, in any other mode of operation the input line is open and will be at 0 V. J12, pin 7 is the LSB input from S4 and is at +5 V dc in LSB, 0 V in any other mode. The inputs at pins 7 and 10 are used in various places on A3 to control the switching between upper and lower sideband. The two inputs are also applied to OR gate U908D to develop a SSB signal when either upper or lower sideband is selected. SPOT ($\overline{SPT}$) input J12 pin 18 is from the front panel SPOT switch S2 and is a ground with the spot button depressed. With the spot button out, the input line is open and pin 16 is at +5 V from pull-up resistor R943. With receive CW operation, a ground at the $\overline{SPT}$ input will enable the 455 and 454.2-kHz oscillators by logic 1's output at J13 pins 12 and 14 and provide the logic 1 at J13 pin 10 to enable the 455-kHz output.

The input to A3 at J20 key interlock not ($\overline{KI}$) pin 3, tune not ($\overline{TUNE}$) pin 1, tune fault not ($\overline{TF}$) pin 2, and key not ($\overline{KEY}$) pin 4 are for future use with an external pa or coupler and should be at logic 1 except for the key line which is tied to J16 pin 15 and will be a logic 0 whenever the key line is low.

J17 pins 2, 3, 4, and 5 are the ground, +14 V and +5 V inputs to A3. J17 pin 1 is an output to the speech processor from A12 pin 14. The input at pin 14 is from the front panel PROC switch, S7D, and is +9 V with the processor ON, 0 V with the processor off.

J12 pin 9 is the AM input from the front panel mode switch and is +5 V with AM operation, 0 V in any other mode.

The CTTL input at J13 pin 39 is from the control card A8. This input is a logic 1 whenever an unauthorized frequency is selected and will disable the transmitter.

$\overline{PTT}$, J12 pin 11, is the input from the VOX circuit and is a logic 0 with a key signal present. $\overline{PTT}$, J16 pin 13, is the push-to-talk input from the front panel mic jack J2 and the rear panel push-to-talk jack J9. Pin 13 is a logic 0 with a push-to-talk signal present.

Loss-of-lock ($\overline{LOL}$), J13 pin 6, is an input from the synthesizer A5 and is a logic 0 when the synthesizer is not in a locked condition. A logic 0 at the $\overline{LOL}$ input disables the transmitter and enables the 5-Hz and 1000-Hz oscillators to produce a beeping tone to indicate a loss of lock.

$\overline{KEY}$ input J16 pin 15 is the key input from the rear panel CW key jack, J10. Pin 15 is logic 0 during a key down condition.

In addition to the control signals generated and used in the A3 board, a number of signals are output for use in other assemblies. J16 pin 3 +9 V dc XMT applies +9 V to the pa during transmit operation to turn on the driver and output stages. This line is at 0 V during receive operation. The PTT output at J12 pin 17 is routed through the front panel vfo select switch S3 to control card A8 where it is used to select the A or B frequency register. Pin 17 is a logic 1 in transmit and a logic 0 in receive.

There is no connection to J16 pin 16, RCVR MUTE.

Amplifier control (AMP CTL) J16 pin 12 is output to J7 on the rear panel where it is available to key an external pa. Pin 12 is ground in transmit, open in receive.

$\overline{PTT}$ J13 pin 32 is a logic 0 in transmit and a logic 1 in receive. This output enables the front panel, passband tuning control in receive and disables it in transmit.

Refer to A3 schematic, sheet 7.

The inputs at J12, pins 1 through 5, are from the front panel bandwidth switch S8. In receive operation +9 V is present on the selected line while the other inputs are at 0 V. During transmit operation all five inputs are at 0 V. The 8.0-kHz, and OPTION 1, 2, and 3 inputs are routed directly through the A3 board to the passband tuning circuit A4. The 2.2-kHz input at pin 2 is ORed with the PTT signal in U908C to select the 2.2-kHz filter in all transmit modes and when 2.2 is selected in receive.

Power reflected (PR) input at J16 pin 8 is an analog dc voltage proportional to reflected power from the directional coupler in the A2 assembly. The PR signal is used in the front panel meter.

The power forward (PF) input at J16 pin 2 is an analog dc voltage proportional to the forward power output from the pa. The signal originates in A2 and is used in the front panel meter.

J16 pin 5, tune power, is an output from the A3 board to the power amplifier. J20 pin 6 is the tune power input to A3 from the remote control interface A14 J2. The tune power control line is for future use with an external pa or coupler.

Band 6, 8, and 9 information is input to A3 at J13, pins 35, 36, and 37 from the control card A8. These inputs are combined with RCV signal to develop four control signals that select the correct high-pass filter during receive operation.

Outputs from the circuits shown on schematic sheet 7, in addition to the previously mentioned filter select outputs include USB XMT, J13 pin 26, LSB XMT, J13 pin 28 and CW SMT, J13 pin 30. Depending on the mode of transmit operation one of these outputs will be at logic 1 while the two unselected modes are at logic 0. The output is used in the passband tuning circuit A4.

The output at J15, PR pin 16, PF pin 12, ALC pin 15, and +14 V dc pin 13 are routed to the front panel METER switch where one is selected for display on the front panel meter during transmit operation. During receive operation switches U901D and U901A are closed and U901B and U901C are opened to route the receive AGC 1 signal to the front panel meter regardless of the METER switch position.

3.4 SELF-TEST

1. The maximum signal amplitude, peak-to-peak, at the output of the peak-to-peak limiter is _____V.

2. What will be the effect on the received signal applied to the mixer U100, pin 1, if L104 opens.

3. With a receive frequency of 3.50000 MHz, relays K_____ and K_____ on the A2A1 filter board of the low pass filter assembly are energized.

4. What is the formula for determining the injection frequency to U100 pin 8.

5. The gain of receive if amplifier Q102 is controlled by the _____ _____ voltage applied to Q102, gate 2.

6. The gain of Q103 is increased during what mode of receive operation?

7. In AM, receive operation, A4J1 pin 11 will be at logic_____.

8. To increase the gain of if amplifier U700, the AGC voltage at pins 3 and 4 must _____.

9. During sideband operation the input to product detector U701, pin 2 is what frequency? _____ kHz.

10. What is the function of variable resistor R622?

3.5 SELF-TEST ANSWERS

1. 13.6 V.
2. If L104 opens, diode switch CR107 is reverse biased, blocking the receive signal to pin 1 of U100.
3. K3 and K8.
4. Receive operating frequency + first if frequency = injection frequency.
5. positive AGC voltage.
6. CW mode.
7. logic 0.
8. decrease.
9. 455 kHz.
10. R622 is the front panel audio output control.

4.1 OBJECTIVES

4.2 BLOCK DIAGRAM ANALYSIS

Figure 4-1

4.3 DETAILED TRANSMIT CIRCUIT ANALYSIS

4.3.1 Transmit Audio Input Circuits

Figure 4-2

4.3.2 VOX Circuit

4.3.3 Speech Processor A12

Figure 4-3

4.3.4 Modulator and Injection Circuits

Figure 4-4
Figure 4-5

4.3.5 Passband Tuning Circuit A4

Figure 4-6

4.3.6 Exciter Mixers, Amplifiers, and ALC

Figure 4-7
Figure 4-8
Figure 4-9

4.3.7 Power Amplifier A1A1

Figure 4-10

4.3.8 PA ALC and Protection Circuits

4.3.9 Low-Pass Filter, T/R Relay and Directional Coupler A2

Figure 4-11

4.4 SELF-TEST

4.5 SELF-TEST ANSWERS

4.1 OBJECTIVES

It is the objective of this section to acquaint the student with the transmit signal flow, beginning with the audio input and ending with the power amplifier output to the antenna. At the conclusion of this section, the student should be able to accomplish the following:

a. Trace the transmit signal through the circuits.
b. Know the assemblies and subassemblies through which the signal passes.
c. Understand the function of each assembly.
d. Understand how the transmit circuits are controlled.
e. Know the operation of each circuit in the transmit signal path.

4.2 BLOCK DIAGRAM ANALYSIS

Refer to the KWM-380 simplified block diagram, figure 4-1. The transmit audio in can be either the front panel mic input or the 600-ohm unbalanced input from the rear panel, J2.

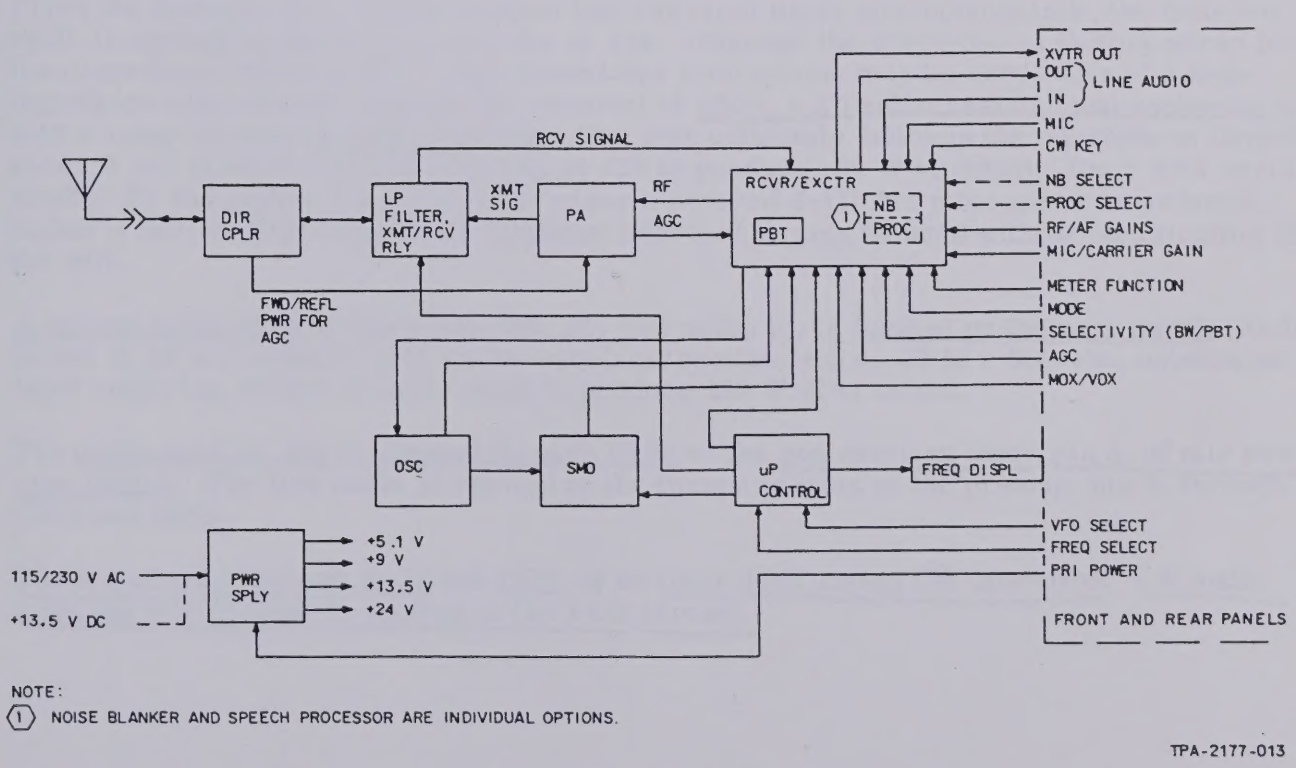


Figure 4-1. KWM-380 Simplified Block Diagram.

Both of these inputs are routed to the mic amplifier on the receiver-exciter A3 board. At the output of the mic amplifier the audio is routed to the VOX circuit and off of the A3 board to the optional speech processor A12. The audio processor provides up to 30 dB of compression of the input audio signal modulation envelope without distortion. With the speech processor a higher level of audio signal can be applied to the exciter modulator to improve "talk power" in the rf output signal. At the output of the processor, A12, the audio signal re-enters the exciter circuits on A3 at J26. In SSB the 455-kHz modulator output and in CW the 455 injection leaves the A3 board at J6 and enters the bandpass tuning circuit A4. The passband tuning circuit provides filtering and determines which sideband will be removed in SSB operation. At the output of A4 the signal again re-enters the A3 circuits. The transmit signal is then mixed to produce the desired operating frequency and applied from A3 to the power amplifier assembly A1. In the A1 module the signal is amplified up to 100 watts, the automatic level control (ALC) is developed and the signal is output to the T/R relay on A2A2. From the T/R relay the signal leaves A2A2 and enters the low-pass filter assembly A2A1.

The signal is filtered and routed back to the directional coupler in the A2A2 assembly. At the output of the directional coupler the rf transmit signal leaves the transceiver at the rf antenna jack on the rear panel.

4.3 DETAILED TRANSMIT CIRCUIT ANALYSIS

The transmit circuits of the KWM-380 will be analyzed by tracing the transmit signal flow, beginning with the mic audio in, to the antenna jack at the output of the power amplifier.

4.3.1 Transmit Audio Input Circuits

Refer to figure 4-2 and the A3 schematic diagram, sheet 4 in the KWM-380 Service Manual.

From the dynamic microphone plugged into the front panel microphone jack, the transmit audio is applied to the exciter circuits at J24. Although the KWM-380 is factory wired for a low-impedance microphone, a high-impedance microphone may be used. Use of a high-impedance microphone requires the removal of R500, a 270-ohm resistor and replacing it with a value between 10 and 47 kilohms that approximately matches the microphone impedance. 5 mV of audio input is required at J24 to produce 100 W rf output. Units with serial number 51 and higher are factory wired for a nominal 3-kilohm microphone impedance. Either a low- or high-impedance dynamic microphone may be used without modification of the unit.

A second audio input to the KWM-380, J1, line audio in, is located on the rear panel. Audio inputs at J2 are routed to J21 on the receiver/exciter board. J2 is a 600-ohm unbalanced input requiring 40-mV of audio input to produce 100 W of rf output.

The audio input at J24 is coupled through C500 to the noninverting input, pin 3, of mic preamp U500A. The line audio is applied to the inverting input of the preamp, pin 2, through C502 and R502.

The signal path through R551 and C550 is an input used during CW operation. CW audio from the mic preamp is applied to the VOX circuit.

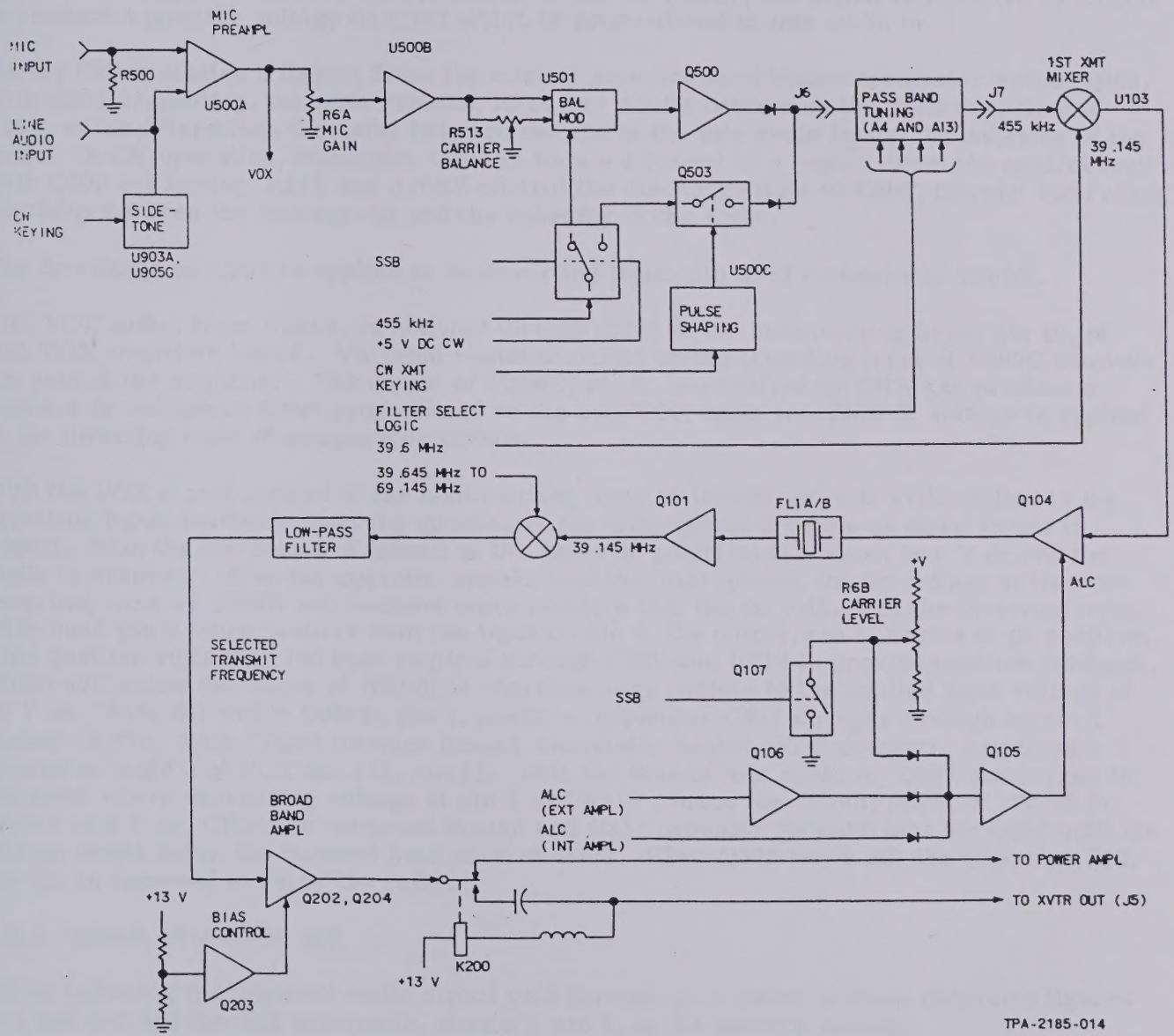


Figure 4-2. Transmit Signal Path Block Diagram.

4.3.2 VOX Circuit

Refer to the A3 schematic, sheet 8.

At the output of mic preamp U500A, pin 1, the audio is coupled through C300 into the VOX circuit. The audio from the mic preamp is applied to the noninverting input of U300D, pin 12. Variable resistor A10R1, VOX gain, on the inverting input of U300D determines the gain of operational amplifier U300D. At the output of U300D, pin 14, the signal is rectified by CR300 to produce a positive voltage on C307 which is proportional to mic audio in.

During SSB operation a logic 1 from the control logic forward biases transistor switch Q301. With Q301 conducting, variable resistor R314 and A10R4 determine the discharge time of C307, which determines the delay between the end of the mic audio in and the unkeying of the radio. In CW operation, transistor Q300 is forward biased by a logic 1 from the control logic. With Q300 conducting, R312 and A10R3 control the discharge time of C307, thereby controlling the delay between the last key-up and the unkeying of the radio.

The dc voltage on C307 is applied to noninverting input, pin 3, of comparator U300B.

Anti VOX audio, from U601A, is coupled through C302 to the noninverting input, pin 10, of anti VOX amplifier U300C. Variable resistor A10R2 on the inverting input of U300C controls the gain of the amplifier. The output of U300C, pin 8, is rectified by CR301 to produce a positive dc voltage on C308 proportional to the anti VOX audio in. This dc voltage is applied to the inverting input of comparator U300B.

With the VOX signal applied to the noninverting input of U300B and anti VOX applied to the inverting input, feedback from the speaker to the microphone appears as equal inputs to U300B. With the two inputs of U300B at the same dc potential the output is 0 V dc and the radio is unkeyed. When the operator speaks into the microphone, the dc voltage at the noninverting input of U300B will become more positive that the dc voltage at the inverting input. With input pin 5 more positive than the input on pin 6, the output, pin 7, begins to go positive. This positive voltage is fed back to pin 5 through C309 and R319 to provide positive feedback, which will cause the output of U300B to increase very rapidly to the applied input voltage of +9 V dc. With the output U300B, pin 7, positive, capacitor C311 charges through forward biased CR302. With CR302 forward biased, transistor switch Q302 conducts, supplying a ground or logic 0 at VOX out J12, pin 12. With the loss of mic audio in, C307 discharges to the point where decreasing voltage at pin 5 of U300B causes the output, pin 7, of U300B to switch to 0 V dc, CR302 is reversed biased and C311 provides forward bias for Q302 until its charge drops below the forward bias point of Q302. When Q302 turns off, the ground at J12, pin 12, is removed to unkey the radio.

4.3.3 Speech Processor A12

While following the transmit audio signal path through A12, refer to block diagrams figures 4-1 and 4-3 and the A12 schematic, sheets 1 and 2, in the service manual.

The optional speech processor, when installed in the KWM-380, is located in the transmit audio signal path, between the mic preamp, U500A and mic gain resistor A10R6B on the A3, receiver/exciter board. The speech processing circuits are enabled by depressing the front panel, PROC, switch. When the PROC switch is not depressed the transmit audio signal is routed directly to mic gain resistor R508, bypassing the processing circuits.

With the PROC switch depressed a logic 1 is applied to the processor board at J1, pin 1. The logic 1 at pin 1 forward biases Q1 and with Q1 conducting Q2 is forward biased. When Q2

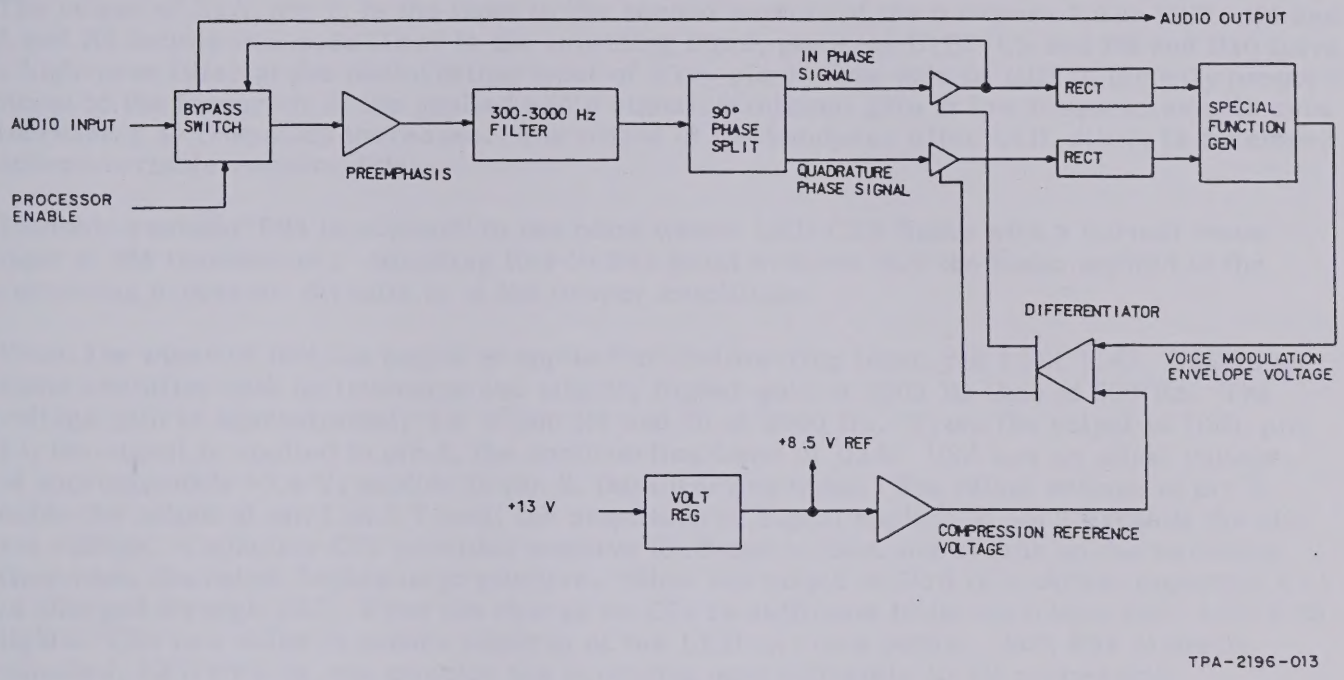


Figure 4-3. Speech Processor Block Diagram.

conducts, the voltage developed across R50, approximately +13 V dc, is applied to U12A, pin 13, and U12B, pin 5, to close both switches. Switch U12C is open at this time.

Audio signal from the mic preamp is applied to the processor at P26 and applied to the noninverting input of U1D, pin 12, through C1, U12A, and R1.

U1D is a preemphasis amplifier. Because of capacitor C46 (in the negative feedback circuit of U1D) as the audio signal increases in frequency the negative feedback decreases which gives the amplifier increased gain at high frequencies.

Because the power (VDC) applied to U1D is +13 V dc and ground, it is necessary to provide a dc offset voltage at the inverting input to make the amplifier operate class A and avoid clipping of the audio signal. The offset voltage for U1D, applied to the junction of R2, R3, and C46 originates at pin 14 of U2D.

The input to U2D, pin 12, is a reference voltage from pin 6 of voltage regulator U11. With the input to U2D applied to the noninverting input and 100 percent negative feedback, pin 14 to pin 13, the dc voltage at pin 14 is equal to the input voltage from U11. While the output of U2D is at approximately +8.5 V dc, it is a common for audio signals because of capacitor C6.

From the output of U1D, pin 14, the audio signal is applied to noninverting input of U1A through R5, R6, and R7. U1A is half of an active audio bandpass filter. U1A and U1B together make up a 300- to 3000-Hz bandpass filter.

R6 and R7, C42 and C3 form a low-pass filter on the noninverting input of U1A. R5 and R6, and C2 form a high-pass filter at the inverting input of U1A. The gain of U1A is inversely proportional to the frequency of the applied audio signal. With gain decreasing as frequency increases, U1A determines the high-frequency cutoff point (3000-Hz) of the bandpass filter. The output of U1A, pin 1, is the input to the second section of the bandpass filter U1B. C4 and 5 and R8 form a low-pass filter to the inverting input, pin 6, of U1B. C5 and R9 and R10 form a high-pass filter at the noninverting input of U1B, pin 5. The gain of U1B is directly proportional to the frequency of the applied audio signal, minimum gain at low frequencies with gain increasing as frequency increases. The output of the bandpass filter U1B, pin 7, is developed across variable resistor R94.

Variable resistor R94 is adjusted to the point where LED CR5 lights with a normal voice input to the transceiver. Adjusting R94 to this point ensures that the audio applied to the remaining processor circuits is at the proper amplitude.

From the wiper of R94 the signal is applied to noninverting input, pin 12 of U3D. U3D is an audio amplifier with no inversion and slightly higher gain at 3000 Hz than at 300 Hz. The voltage gain is approximately 8.6 at 300 Hz and 10 at 3000 Hz. From the output of U3D, pin 14, the signal is applied to pin 3, the noninverting input of U3A. U3A has an offset voltage, of approximately +7.4 V, applied to pin 2, the inverting input. The offset voltage at pin 2 holds the output at pin 1 at 0 V until the amplitude of signal applied to pin 3 exceeds the offset voltage. Capacitor C50 provides positive feedback to U3A and speeds up the switching time when the output begins to go positive. When the output of U3A is positive, capacitor C51 is charged through R95. When the charge on C51 is sufficient to forward bias Q10, LED CR5 lights. C51 is a delay to reduce blinking of the LED on voice peaks. With R94 properly adjusted, LED CR5 on, the circuits are providing approximately 15 dB processing.

From variable resistor R94 the main signal path is to the noninverting inputs of U2B and U2C. U2B and U2C are buffer amplifiers with unity gain. The output of U2C, pin 8, and U2B, pin 7, which are in phase are applied to a 90 degree phase shift network. One output of the phase shift network is applied to the noninverting input, pin 5, of U3B, the second output of the phase shifter is applied to the noninverting input, pin 10 of U3C. The signals applied to U3B and U3C have a 90 degree phase difference, with the signal at U3B being the I or In phase channel and the signal at U3C the Q or Quadrature (90 degree phase shift) channel. U3B and U3C are both noninverting, unity gain buffer amplifiers.

The I channel audio from U3B, pin 7, is applied to the noninverting input of U4A and the Q channel audio from U3C, pin 8, is applied to the noninverting input of U4D. U4A and U4D are matched, transconductance, operational amplifiers with external gain control at pins 1 and 16. As the current to pins 1 and 6 increases, the output amplitude of the signal increases and as the current decreases the output amplitude decreases. The amount of AGC applied to U4A and U4D is determined by the processor (compressor) circuit and adjusted to keep the audio out of the processor card at the optimum level.

The outputs of U4A and U4D are applied to buffer amplifiers U4B and U4C. The outputs of U4B and U4C, pins 8 and 9 are applied to transistor amplifier Q8 and Q9 through C18 and C19. The signal at the emitter of Q8 (TP1) is the audio output of the audio speech processor card. From TP1 the signal is coupled through C43 to output level adjustment R31. From R31 the signal is routed through switch U12B to the output at J26.

The I channel signal at TP1 and the Q channel signal at TP2 are equal in frequency and amplitude with a phase difference of 90 degrees. By applying the two signals to a scope, one to the horizontal input and one to the vertical input, the signals can be checked for proper frequency, amplitude, and phase relationship. When the signals at TP1 and TP2 are correct, the Lissojous figure on the scope will be a perfect circle.

The I channel signal at the collector of Q8 is coupled through C20 and applied to a precision full-wave rectifier made up of U5, U6, and their associated components. The rectifier produces a positive dc voltage at U6, pin 6, that is proportional to the instantaneous amplitude of the I channel signal.

The Q channel signal at the collector of Q9 is applied to precision full-wave rectifier U7, U8, and associated components. The output at U8, pin 6 is a positive dc voltage proportional to Q channel audio amplitude.

The output of the I channel rectifier is applied to current inputs 1 and 2 (I_1 and I_2) of analog multiplier U10. The output of the Q channel rectifier is applied to the noninverting input of U9A, pin 3 and the noninverting input of U9B, pin 5. The output of U9B pin 7 is also applied as an input to U9A. The output of U9A, pin 1, is applied to current input 3 (I_3) of U10.

U9A, B, D, U10, and their associated components make up a trigonometric function generator. The trigonometric function generator squares each of the output signals of the rectifiers, adds them together, and takes the square root of the sum. The function generator output (TP3) is a signal whose amplitude varies only as the amplitude of the input audio signal.

The output of the function generator U9B, pin 7, is applied to the base of Q7. Q7 and Q6 are a differentiator with the output taken from the collector of Q6. The input to the base of Q6 is a dc reference voltage from U9C. The input at pin 10 of U9C is a regulated +8.5 V dc. Resistive voltage divider R55 and R56 set the gain of U9C at approximately 0.1 giving an output voltage at pin 8 of +0.85 V dc. Because the input to Q6 is constant the input to Q7 will control the output of the differentiator.

When the output of U9B increases the forward bias of Q7 is increased, decreasing the conduction of Q6, which decreases the conduction of Q5, Q4, and Q3. As the conduction of Q5 and Q4 decrease, the current controlling the gain of U4A and U4D decreases, lowering the gain of the amplifiers. When the output of U9B increases the above sequence in reversed to increase the gain of U4A and U4D. By varying the AGC to compress the audio peaks, a higher-level signal can be input to the processor to raise the level of the valleys. This produces a higher average signal level to increase the "talk power" in the transmitter rf output signal.

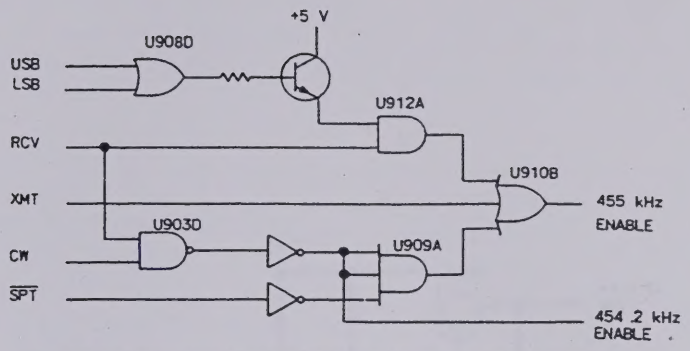
U11 is an integrated circuit regulator that provides +8.5 V dc to various circuits on the audio speech processor card. The input to U11 is from J1, pin 3, and is the regulated +14-V dc from the KWM-380 power supply. R52, at the output, pin 10, of U11 is a current sense resistor that determines the maximum current output. R54 and R53 are selected to produce the desired +8.5 V dc output. If the output voltage of U11 varies, the error is sensed by R53 and R54 and a portion of the error is applied to the inverting input, pin 4, to correct the error.

When the processor circuits are disabled, J1, pin 1, at logic 0, Q1 and Q2 are reverse biased and the +13-V dc at the collector of Q1 is applied to U12C to close the switch. The logic 0 at the emitter of Q2 keeps U12A and U12B open. This routes the input signal from P26 through C49 and U12C to the output at J26, bypassing the processor circuits.

The output of A12 is applied to J26 on the A3 board.

4.3.4 Modulator and Injection Circuits

Refer to figures 4-4 and 4-5 in the self-study manual and the A3 schematic, sheets 4 and 5 in the service manual.



	USB	LSB	CW	AM	SPT	KI	TXI	PTT	TUNE	LOL	TF	KEY	XMT	RCV
455 kHz ENABLE =0	0	0	0	-	X	-	-	-	-	-	-	-	0	X
	X	X	X	-	1	-	-	-	-	-	-	-	0	0
455 kHz ENABLE =1	X	X	X	-	X	-	-	-	-	-	-	-	1	X
	1	X	X	-	X	-	-	-	-	-	-	-	X	1
	X	1	X	-	X	-	-	-	-	-	-	-	X	1
	X	X	1	-	0	-	-	-	-	-	-	-	X	1
454.2 kHz ENABLE =1	-	-	1	-	-	-	-	-	-	-	-	-	-	1
=0	-	-	1	-	-	-	-	-	-	-	-	-	-	0
=0	-	-	0	-	-	-	-	-	-	-	-	-	-	1

1= LOGIC 1 X= DON'T CARE
0= LOGIC 0 -= NOT APPLICABLE

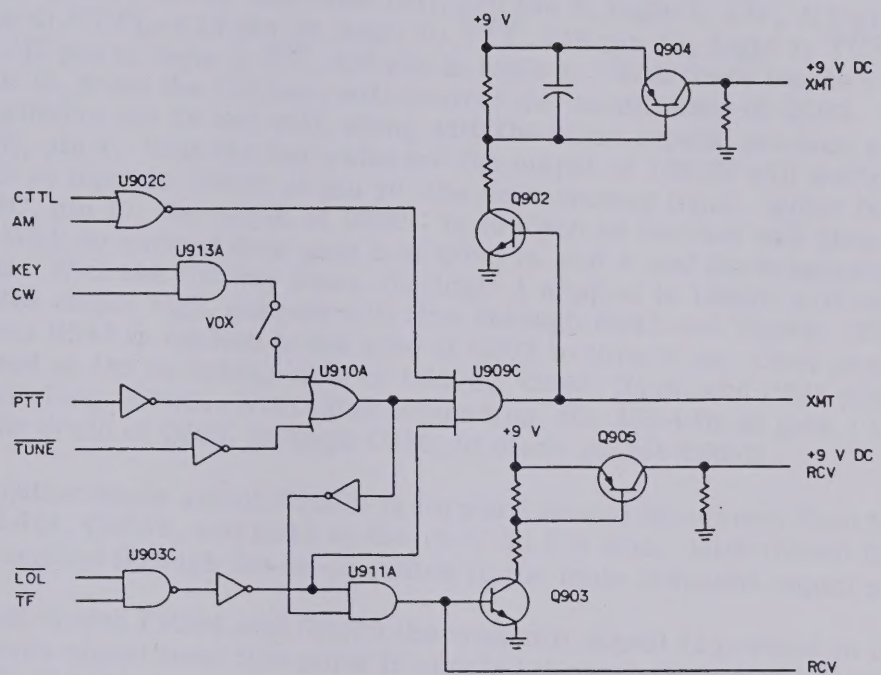
TPA-2182-013

Figure 4-4. BFO Enable Simplified Logic Diagram and Chart.

The output of mic preamp, U500A, pin 1, is routed through speech processor A12 to variable resistor A10R6B, mic gain. Mic gain is a front panel control that adjusts the level of audio input to the modulator during sideband operation. From gain control resistor A10R68 the transmit audio is coupled through C505 to amplifier U500B pin 5. From the output of U500B the signal is coupled through C509 to the signal inputs, pins 1 and 4, of balanced modulator U501. Variable resistor R513 is the carrier balance adjust for the modulator. The 455-kHz carrier input to the balanced modulator is applied to pins 8 and 10.

The 455-kIIz for the modulator is input from the oscillator assembly, A7, to the exciter circuits at A3J10, at approximately 100 mV. The signal is coupled through C517 to the junction of diodes CR500 and CR501. During transmit operation diode switch CR500 is forward biased by current flow from ground through R525, L503, CR500, L502, and L501 to the +5-V dc xmt line. The injection signal path is through CR500 and C521 to the junction of CR502 and CR503. During sideband operation CR502 is forward biased by current flow from ground through R526, L506, CR502, and L509 to the +5-V dc SSB line. CR503 is off with SSB operation. In sideband operation with audio input applied, the output of balanced modulator U501 pin 6 is a 455-kIIz amplitude modulated signal. This signal is applied to the base of common emitter amplifier Q500, amplified and coupled from the collector of Q500 through C514 to diode switch CR508. During sideband operation CR508 is forward biased by current flow from ground through R547, L514, CR508, and L513 to the +5-V dc SSB line passing the signal through CR508.

During CW operation the 455-kIIz input at A3J10 is routed through diode CR500, CR503, C528, and R552 to gate 1 of Q503. CR503 is enabled during CW operation by current flow



	USB	LSB	CW	AM	SPT	KI	CTTL	PTT	TUNE	LOL	TF	KEY
XMT (AND +9 V DC XMT) =0	-	-	X	X	-	-	1	X	X	X	X	X
	-	-	X	1	-	-	X	X	X	X	X	X
	-	-	X	X	-	-	X	X	X	0	X	X
	-	-	X	X	-	-	X	X	X	X	0	X
	-	-	0	X	-	-	X	1	1	X	X	X
	-	-	X	X	-	-	X	1	1	X	X	0
*	-	-	X	X	-	-	X	1	1	X	X	X
XMT (AND +9 V DC XMT) =1	-	-	X	0	-	-	0	X	0	1	1	X
**	-	-	X	0	-	-	0	0	X	1	1	X
	-	-	1	0	-	-	0	X	X	1	1	1
RCV (AND +9 V DC RCV) =0	-	-	X	-	-	-	-	X	X	0	X	X
	-	-	X	-	-	-	-	X	X	X	0	X
	-	-	X	-	-	-	-	X	0	X	X	X
	-	-	X	-	-	-	-	0	X	X	X	X
**	-	-	1	-	-	-	-	X	X	X	X	1
RCV (AND +9 V DC RCV) =1	-	-	0	-	-	-	-	1	1	1	1	X
	-	-	X	-	-	-	-	1	1	1	1	0
*	-	-	X	-	-	-	-	1	1	1	1	X

1= LOGIC 1 X= DON'T CARE
0= LOGIC 0 -= NOT APPLICABLE
* VOX SW OPEN ** VOX SW CLOSED

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Figure 4-5. +9 V dc XMT and RCV Simplified Logic Diagram and Chart.

from ground through R529, L566, CR503, and L507 to the +5-V dc CW line. Q503 is an N-channel, dual gate, depletion type, insulated gate, field effect transistor. While the 455-kHz is applied to gate 1 of Q503, the dc voltage present at gate 2 determines when Q503 is allowed to conduct.

To see how Q503 is enabled during CW, transmit operation it is necessary to look at the control circuitry shown on the A3 schematic, sheet 6. During CW transmit operation the inputs that will control Q503 are; key interlock ($\overline{KI}$), J20 pin 3, logic 1; CW, J12 pin 8, logic 1; AM, J12 pin 9, logic 0; CTTL, J13 pin 39, logic 0; $\overline{PTT}$, J16 pin 13, logic 1; $\overline{TUNE}$, J20 pin 1, logic 1; $\overline{LOL}$, J13 pin 6, logic 1; $\overline{TF}$, J20 pin 2, logic 1. With these inputs present the $\overline{KEY}$ input at J16 pin 15, from the CW key, will control the on-off state of Q503. With the key down, a logic 0 is applied to pin 16 and will, along with the other inputs, produce a logic 1 at the output of U902B, pin 4. With the key released the output of U902B will switch to logic 0. The output of U902B is input to U500C at pin 10, the noninverting input. Refer to sheet 4. With a logic 0 at U500C, pin 10, the output of U500C is low and no current will flow through zener diode VR500. With no current flow gate 2 of Q503 is at 0 V and the transistor is off, blocking the 455-kHz. With the CW key down, the logic 1 applied to U500C will cause the output to go high. With the output high, current will flow through R542 and VR500. The voltage developed across R542 is applied to the gate of Q503 to turn it on. C544 provides positive feedback to speed up the switching time of U500C. C545, R548, and R549 prevent noise pulses from switching U500C. With Q503 conducting, the 455-kHz at gate 1 is amplified and coupled from the drain of Q503, through C540, to diode switch CR509.

During CW operation diode switch CR509 is forward biased by current flow from ground through R547, L514, CR509, and L515 to the +5-V dc CW line. With CR509 forward biased the 455-kHz is applied through the diode switch to the main transmit signal path.

At the junction of diodes CR508 and CR509 the transmit signal is present in SSB or CW operation. The transmit signal from this point is coupled through C548 to diode switch CR116. Refer to sheet 3. CR116 is forward biased during transmit operation by current flow from ground through R123, CR116, L128, and L127 to the +9-V dc xmt line. The signal, after passing through CR116, is blocked by reverse biased CR115 and is routed through C152 to A3J6. At J6, the transmit signal exits the receiver/exciter board and enters the variable if (passband tuning circuit A4).

4.3.5 Passband Tuning Circuit A4

Refer to figure 4-6 in the self-study manual and the passband schematic, sheets 1 and 2, in the service manual.

The 455-kHz signal enters the passband tuning circuit at A4J3. From J3 the signal is applied to pin 1 of mixer U4, through a low-pass filter comprised of L1, C1, and C2. The second input to the mixer, pin 8 is the output of crystal oscillator Q2, applied through amplifiers Q3 and Q4. Refer to sheet 2.

The frequency of oscillator Q2 is determined by the Y1 crystal frequency, variable capacitor C16 and the voltage applied to voltage variable capacitor CR13. The dc voltage applied to the cathode of CR13, through R56 and R40 is from switch U1A, U1B, or U1C depending on the mode of operation.

During upper sideband, transmit operation, J1 pin 10, UPPER, is at a logic 1 while J1 pins 14, 12, and 16 are at logic 0. The logic 1 at J1, pin 10, is applied to the noninverting input of voltage comparator U3A, pin 5. The output stage of U3A is an uncommitted collector of a grounded emitter NPN output transistor. With a logic 1, approximately +5 V, at input pin 5

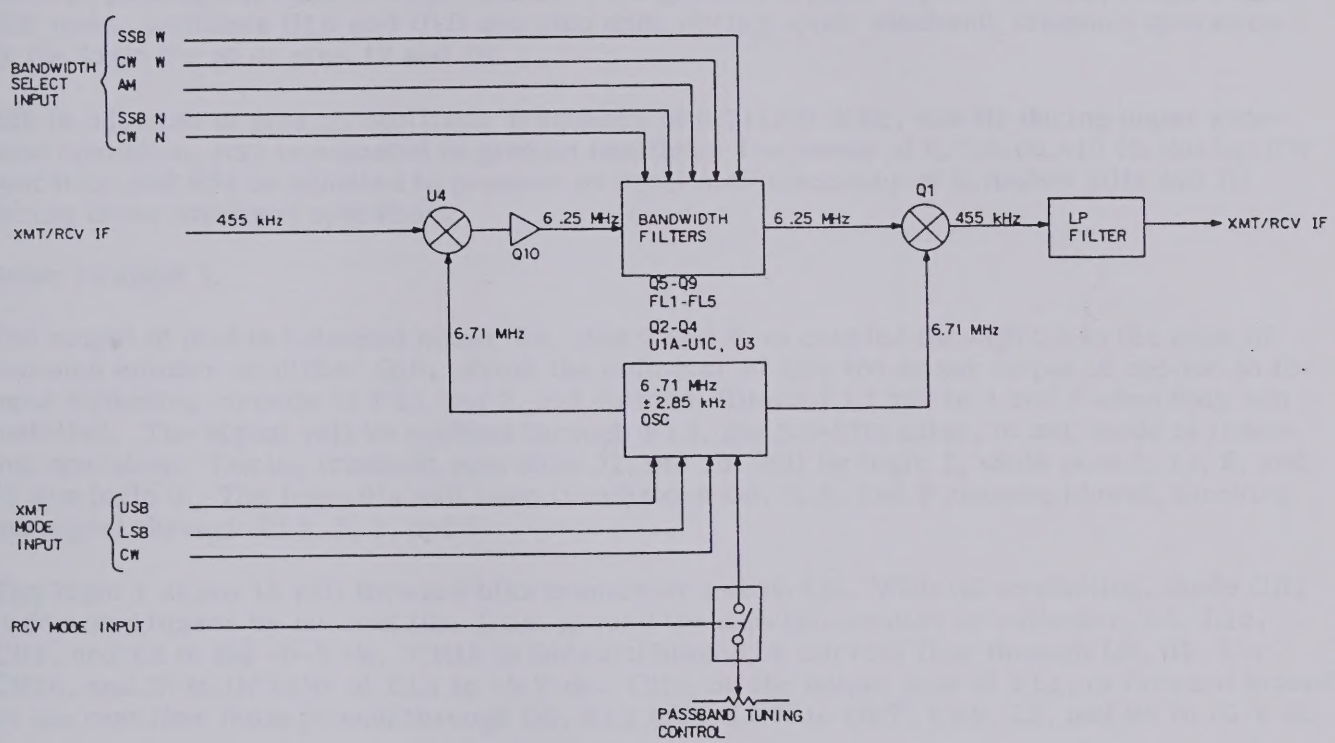


Figure 4-6. Passband Tuning Block Diagram.

and approximately 1 V at input pin 4 the output transistor in U3A in reverse biased. With the output stage reverse biased, U3A output, pin 2, goes to +18 V from pull-up resistor R61. The +18 V at U3A, pin 2, is applied to pin 6 of COS/MOS bilateral switch U1C. The minimum voltage at pin 6 required to close switch U1C is +15 V dc. With switch U1C closed, the voltage on the wiper of variable resistor R28 (in resistive voltage divider R36, R34, R35, R31, R32, R28, R29, and R27) is applied to CR13.

The logic 0 at J1, pin 14, is applied to pin 7 of U3B. The inverting input of U3B, pin 6, is held at +1 V dc by voltage divider R59 and R60. With these inputs the output stage of U3B is conducting, placing a ground at output pin 1. This ground, applied to pin 5 of U1B, keeps switch U1B open. Switches U1A and U1D are also upon during upper sideband, transmit operation by the logic 0's at J1 pins 12 and 16.

R28 is adjusted to give an oscillator frequency of 6.711500 MHz, ±10 Hz during upper sideband operation, R31 is adjusted to give an oscillator frequency of 6.710000 ±10 Hz during CW operation and R34 is adjusted to produce an oscillator frequency of 6.708500 MHz ±10 Hz during lower sideband operation.

Refer to sheet 1.

The output of double balanced mixer U4, pins 3 and 4, is coupled through C3 to the base of common emitter amplifier Q10. From the collector of Q10 the mixer output is applied to the input switching circuits of FL1 and 3, and optional filters FL2 and to 4 and 5 when they are installed. The signal will be enabled through FL1, the 2.2-kHz filter, in any mode of transmit operation. During transmit operation J1, pin 13, will be logic 1, while pins 9, 11, 8, and 15 are logic 0. The logic 0's will keep transistors Q6, 7, 8, and 9 reverse biased, blocking the signal through FL2, 3, 4, and 5.

The logic 1 at pin 13 will forward bias transistor switch Q5. With Q5 conducting, diode CR1 is forward biased by current flow from ground through Q5, emitter to collector, R2, L10, CR1, and L2 to the +5-V dc. CR16 is forward biased by current flow through Q5, R2, L10, CR16, and IN to IN LOW of FL1 to +5 V dc. CR2, on the output side of FL1, is forward biased by current flow from ground through Q5, FL1 OUT LOW to OUT, CR2, L3, and R7 to +5 V dc.

With diodes CR1, CR16, and CR2 forward biased, the signal is routed through SSB filter FL1. From the output of the filter, the signal, nominally 6.255-MHz, is applied to gate 1 of Q1 through high-pass filter C23, C24, L4, and R24. Refer to sheet 2. Q1 is the second mixer in the passband tuning circuit. The second input to the mixer on gate 2, is the nominal 6.71-MHz from oscillator Q2 through Q3. Variable Resistor R65 is the gain adjustment for mixer Q1.

Filter FL1 has a 2.2-kHz bandpass with a center frequency of 2.255 MHz. With USB transmit operation, the output of mixer U4 will be centered at 6.711500 MHz - 455 kHz or 6.256500 MHz. The bandpass of the filter is 2.2 K centered at 6.255 or from 6.253900 to 6.256100 MHz. This puts the carrier frequency and the lower sideband outside of the filters bandpass.

For CW operation the carrier would be centered in the filters bandpass and in LSB transmit operation the carrier and upper sideband would fall below the filters bandpass.

The output of mixer Q1 is filtered by low-pass filter C29, C53, C30, C40, C41, L6, L16, L17, and L18. The output of the filter, nominally 455 kHz, leaves the passband tuning circuit at A4J6 and enters the receiver/exciter board at A3J7.

4.3.6 Exciter Mixers, Amplifiers and ALC

Refer to figures 4-7, 4-8, and 4-9 in the self-study manual and the exciter schematics, sheets 1, 2, and 3 in the service manual.

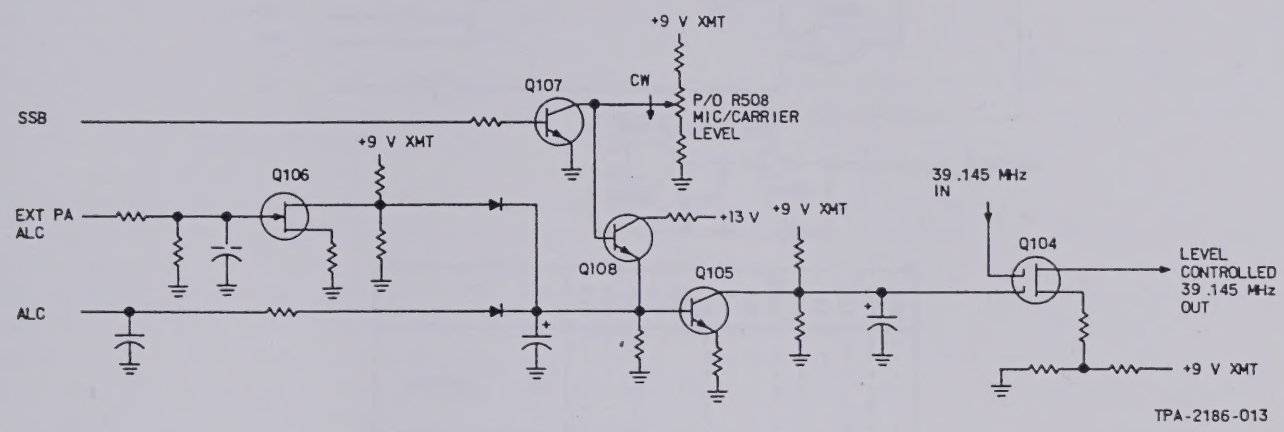
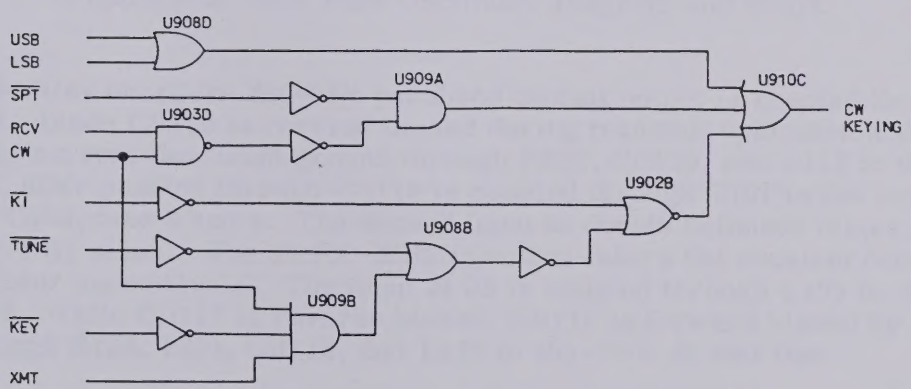


Figure 4-7. Exciter ALC Simplified Diagram.



	USB	LSB	CW	AM	SPT	KI	TXI	PTT	TUNE	LOL	TF	KEY	XMT	RCV
CW KEYING =0	CW KEYING=0 UNDER ALL CONDITIONS EXCEPT FOR CW KEYING = 1 BELOW.													
CW KEYING =1	1	X	X	-	X	X	-	-	X	-	-	X	X	X
	X	1	X	-	X	X	-	-	X	-	-	X	X	X
	X	X	1	-	0	X	-	-	X	-	-	X	X	1
	X	X	X	-	X	1	-	-	1	-	-	X	X	X
	X	X	1	-	X	X	-	-	X	-	-	0	1	X

1= LOGIC 1 X= DON'T CARE
0= LOGIC 0 -= NOT APPLICABLE

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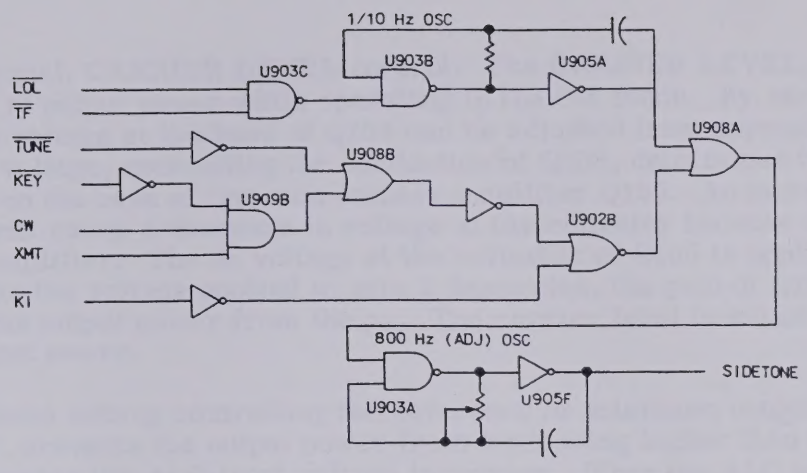
Figure 4-8. CW Keying Logic Diagram and Chart.



	USB	LSB	CW	AM	SPT	KI	TXI	PTT	TUNE	LOL	TF	KEY	XMT	RCV
SIDETONE =0	-	-	0	-	-	X	-	-	1	1	1	X	X	-
	-	-	0	-	-	0	-	-	X	1	1	X	X	-
	-	-	X	-	-	X	-	-	1	1	1	1	X	-
	-	-	X	-	-	0	-	-	X	1	1	1	X	-
	-	-	X	-	-	X	-	-	1	1	1	X	0	-
	-	-	X	-	-	0	-	-	X	1	1	X	0	-
SIDETONE =1 (PULSED)	-	-	X	-	-	X	-	-	X	0	X	X	X	-
	-	-	X	-	-	X	-	-	X	X	0	X	X	-
(CONSTANT UNLESS TF OR LOL=0)=1	-	-	X	-	-	1	-	-	0	•	•	X	X	-
	-	-	1	-	-	X	-	-	X	•	•	0	1	-

1=LOGIC 1
0=LOGIC 0

X=DON'T CARE
-=NOT APPLICABLE
•=SIDETONE PULSED IF TF OR LOL=0

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Figure 4-9. Side Tone Oscillator Diagram and Chart.

From J7 on the exciter board the 455-kHz passband circuit output is coupled through C158 shown on sheet 3. Diode CR120 is reverse biased during transmit operation while CR119 is forward biased by current flow from ground through R125, CR119, and L113 to the +9-V dc xmt line. The signal, after passing through CR119 is coupled through C161 to the input of the first transmit mixer, U103, pins 3 and 4. The second input to double balanced mixer, U103, pin 8, is a fixed 39.600-MHz signal. The 39.600-MHz injection enters the receiver/exciter board at J3 from oscillator assembly A7. The input at J3 is coupled through C155 to the junction of CR117 and CR118. While CR117 is reverse biased, CR118 is forward biased by current flow from ground through R124, L131, CR118, and L132 to the +9-V dc xmt line.

The output of the first transmit mixer U103, pin 1, is 39.145 MHz and is applied to gate 1 of transmit if amplifier Q104 through high-pass filter, C164, C162, and L135. Variable inductor L135 is adjusted to remove the 455-kHz component from the output of mixer U103.

Refer to sheet 2.

The input to gate 2 of transmit if amplifier Q104 is the automatic level control voltage (ALC). The ALC signal originates, either in the forward power detector of the KWM-380 or an external power amplifier such as a 30L-1 linear amplifier. The internal ALC enters the receiver/exciter board at J16, pin 6, while the external ALC enters at J16, pin 14.

Following is an explanation of the ALC circuits on the receiver/exicter board with CW operation using an external power amplifier. With CW operation, a logic 0 from the control logic applied to the base of transistor switch Q107. The logic 0 reverse biases Q107 which

enables the front panel, CARRIER LEVEL control. The CARRIER LEVEL control is used to adjust the desired rf output power while operating in the CW mode. By varying the carrier level resistor, the voltage at the base of Q108 can be adjusted from approximately 1.0 V dc to 2.0 V dc. This voltage, controlling the conduction of Q108, determines the minimum or reference voltage on the base of common emitter amplifier Q105. An increase in voltage at the base of Q105 will cause a decrease in voltage at the collector because of the phase inversion through the amplifier. The dc voltage at the collector of Q105 is applied to gate 2 of amplifier Q104. As the voltage applied to gate 2 decreases, the gain of Q104 is lowered, which will lower the output power from the pa. The carrier level is adjusted to establish the desired rf output power.

With the carrier level setting controlling the reference or minimum output power, the ALC input at J16, pin 6, prevents the output power from increasing higher than the desired level. As power out increases the ALC input voltage increases. When the ALC input voltage increases to a higher level than the voltage at the base of Q108, CR122 is forward biased, charging C175 to the higher level. This will increase in the forward bias of Q105 and will cause a decrease in the collector voltage which is applied to gate 2 of Q104 to lower the gain of Q104. The gain of Q104 is reduced, reducing the rf output power until the ALC input at J16, pin 6, drops below the base voltage of Q108.

With an external power amplifier, the ALC developed in the external amplifier is fed back to the KWM-380 and enters the receiver/exciter board at J16, pin 14. The input at J16, pin 14, is a negative dc voltage that is directly proportional to the rf power out. As the external amplifiers rf output power increases, the increasingly negative dc voltage applied to the gate of Q106 reduces the conduction of Q106. As the conduction of Q106 decreases the drain voltage applied to CR125 increases. If the voltage at the anode of CR123 exceeds the base voltage of Q108 or the anode voltage of CR133, CR123 will forward bias and C175 will charge to the new higher voltage. The increase in voltage at C175 will decrease the gain until external ALC sample reverse biases CR123 and CR125.

During sideband operation, a logic 1 applied to the base of Q107, forward biases Q107. With Q107 forward biased, a ground is applied through Q107 to the base of Q108 keeping the transistor reverse biased and removing the CARRIER LEVEL adjust from the circuit.

From the drain of transmit if amplifier Q104 the transmit signal path is through R130 and C173 to T/R diode switch CR113. CR113 is forward biased during transmit operation by current flow from ground through R111, R121, CR113, L139, L137, and L138 to the +9-V dc xmt line.

The signal, after passing through CR113, is blocked by reverse biased CR114 and coupled through C133 to the 39.145-MHz crystal filter FL1A/B. Variable inductor L120 is adjusted to provide impedance matching at the input of the filter. Crystal filter FL1A/B is an 8-kHz bandwidth filter used to remove the 39.600-MHz component from the output of the mixer. L119 provides impedance matching at the filter output. The 39.145-MHz transmit if is coupled through C132 and C130 to the junction of diodes CR111 and CR112. During transmit operation, CR111 is reverse biased while CR112 is forward biased by current flow from ground through R109, L118, CR112, and L117 to the +9-V dc xmt line. The signal, after passing through CR112 is coupled through C127 to the source of grounded gate amplifier Q101. Q101 is a broadband, low-noise amplifier with a low-input impedance and a high-output impedance. Variable inductor L110 is adjusted for impedance matching at the output of Q101. From the drain of Q101 the 39.145-MHz transmit if signal is coupled through C119 to the anode of CR109. CR109 is forward biased during transmit operation by current flow from ground through R106, L108, CR109, and L109 to the +9-V dc xmt line. The signal, after passing through CR109, is blocked by reverse biased CR110 and coupled through C115 to the second transmit mixer, pins 3 and 4.

Refer to sheet 1.

The second input to mixer U100 is the variable injection from loop 1 in the synthesizer, entering the receiver/exciter board at J2 and entering the mixer at pin 8. The input signal at J2 ranges from 40.94500 MHz, with a dial frequency of 1.80000 MHz to 68.84500 MHz with a dial frequency of 29.70000 MHz. The injection signal applied to U100, pin 8, is approximately +17 dB and can change in 10-Hz steps. The injection frequency, minus the transmit lst if frequency is equal to the dial transmit frequency.

The output of the second transmit mixer, pin 1, is filtered by low-pass filter C111, C114, L107, C110, C113, L106, C108, C109, C112, L015, C107, and C106. This filter is a 30-MHz low-pass filter which removes the 39.14500-MHz and variable injection components from the mixer output while coupling the difference frequency, 1.80000 to 29.70000 MHz to the junction of CR107 and CR108. During transmit operation CR107 is reverse biased while CR108 is forward biased by the current flow from ground through R105, L104, CR108, and L103 to the +5-V dc xmt line. After passing through CR108 the transmit signal is coupled through C200 and C208 to the base of broadband amplifier Q202. Refer to sheet 2. L203 and R216 provide a path for negative feedband in the amplifier. Transistor Q202 is forward biased during transmit operation by the +9-V dc xmt applied to L206 and reverse biased during receive operation.

From the collector of Q202 the signal is coupled through C212 and C213 to the base of the output broadband amplifier Q204. Q203 provides temperature compensated, emitter-base, bias current for Q204. During transmit operation an increase in temperature at the emitter-base junction of Q203 will cause the base-emitter resistance to decrease and the forward bias current to increase. The tendency of Q203 conduction to increase with temperature, is counteracted by diode CR200. Any temperature increase affecting Q203 will also be felt by CR200, causing the resistance of CR200 to decrease and the voltage drop across CR200 to decrease. If the voltage across CR200 decreases, the voltage drop across R217 (on the base of Q203) will increase to keep the bias level of Q203 constant. With no signal applied, forward bias for Q204 is, from ground through R222, the emitter-base junction of Q204, R219, collector to emitter of Q203 and R221 to the +14-V dc. Negative feedback from the collector of Q204, through R223 to the junction of C212 and C213 reduces distortion and the possibility of oscillations in the amplifier stage. The output of the final exicter broadband amplifier is coupled through C217 to relay K200. In the deenergized condition (shown on schematic) relay K200 routes the signal to the power amplifier through J1. With K200 energized, by a ground through a 1 MH choke at the rear panel XVTR jack, the signal is coupled through C218 to J8. Q202 and 203 combined have a gain of approximately 23 dB to produce a 100-mW output from the exciter.

4.3.7 Power Amplifier A1A1

Refer to pa block diagram figure 4-10 in the self-study manual and the pa schematic A1 in the service manual.

The transmit rf input to the power amplifier, A1, enters A1 at P1 from the receiver/exciter board. The frequency of the input signal at P1 ranges from the 160-through the 10-M amateur bands and can vary in 10-Hz steps. The level of the rf input to the pa ranges from 10-to-100 MW depending on frequency and operating power.

The pa input circuit consisting of R1, R2, C1, L1, R15, and C8 provides impedance matching between the output of the exciter and the predriver, Q1 in the pa. The nominal 100-mW input signal to the pa is applied to the base of common emitter, predriver, Q1. Bias current for Q1 is provided by Q4. During normal operation the positive dc output voltage from U101A

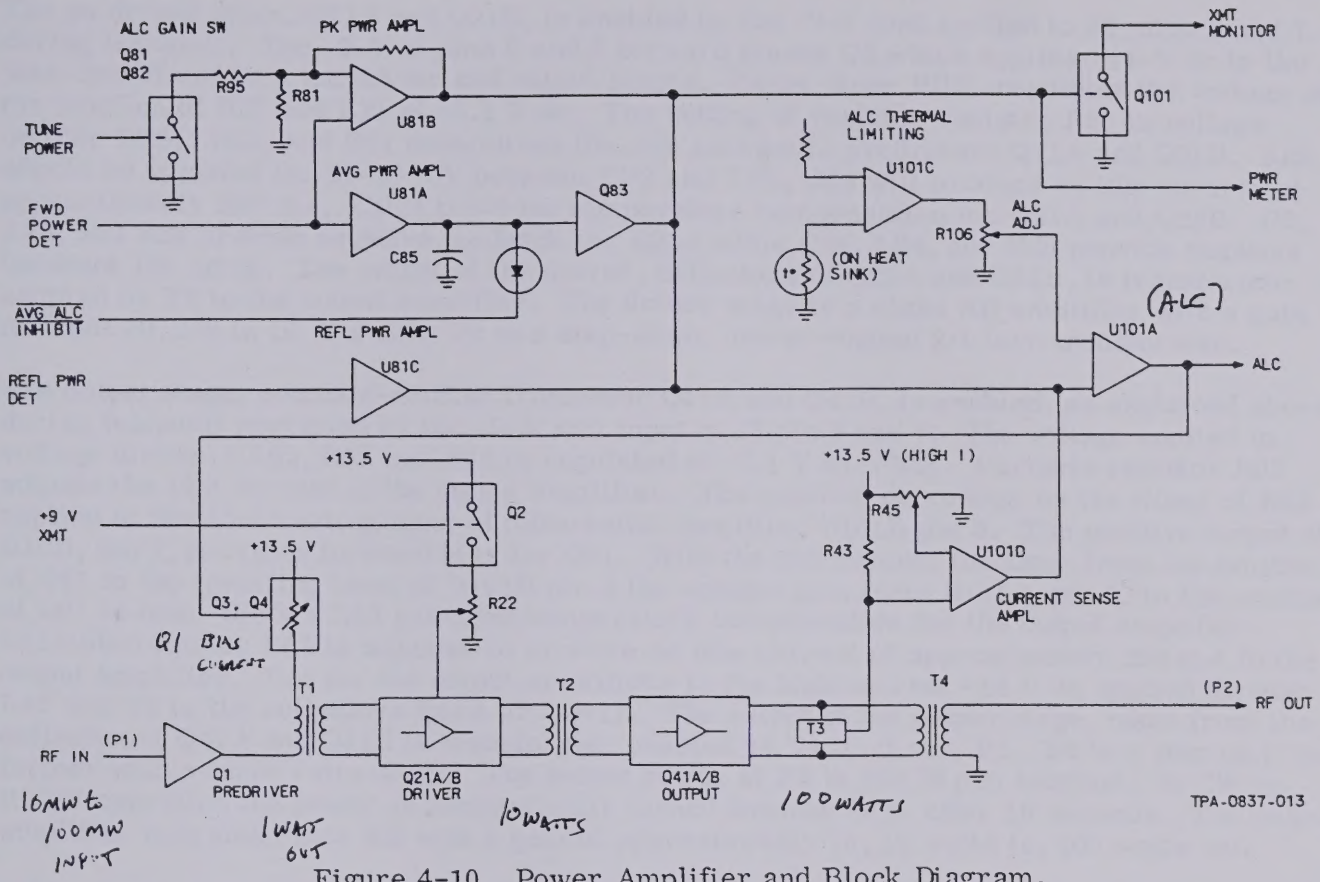


Figure 4-10. Power Amplifier and Block Diagram.

(ALC) is not sufficiently high to forward bias CR2 through VR1. With no current flow through CR2, Q3 is reverse biased. With Q3 off, Q4 provides maximum forward bias for Q1. The gain control required to maintain the desired RF output level from the pa is accomplished on the A3 board using the ALC output of U101A. If the ALC line to A3 is broken or disabled, or if the pa is operated on a test fixture the ALC from U101A to CR2 offers protection against excessive output power. As pa output power increases to an abnormally high level the ALC voltage applied to CR2 will increase to the point where CR2 is forward biased through VR1. With current flow through VR1 and CR2, Q3 begins to forward bias. With Q3 conducting, R12 and the emitter-collector resistance of Q3 form a voltage divider with R11 on the base of Q4. This voltage divider reduces the forward bias and conduction of Q4. As the conduction of Q4 decreases, the forward bias and gain of Q1 is reduced to lower the pa output to a safe level. Q1 is a class A amplifier and normally operates with a gain of approximately 10, 100 mW in for 1 W out. Because the frequency response of both the predriver and driver stages is not flat, frequency compensation networks in both stages increase their gain as frequency increases.

Diode CR1 on the base of Q1 provides temperature compensation for the predriver. As the temperature of the circuit increases, the emitter-base resistance of Q1 decreases, increasing the forward bias. This increase in temperature also decreases the resistance of CR1, and the voltage drop across CR1 decreases to reduce the forward bias of Q1, which keeps conduction constant. The output at the collector of Q1 is transformer-coupled by T1 to the input of the driver stage. T1 is a step down 3:1 center-tapped transformer.

The pa driver stage, Q21A and Q21B, is enabled by the +9-V xmt applied to J3, pins 5 and 7, during transmit. The +9-V at pins 5 and 7 forward biases Q2 which applies +14-V dc to the bias circuits of both the driver and output stages. Zener diode VR21 regulates the voltage at the junction of R27 and R21 at +5.1 V dc. The setting of variable resistor R22 in voltage divider CR21, R22, and R21 determines the idle current in predrivers Q21A and Q21B. R22 should be adjusted for 27-29 mV between TP2 and TP3, this will produce an idle current of approximately 250 mA. CR21 provides temperature compensation for Q21A and Q21B. C3, L23, and R25 provide negative feedback for Q21A while C24, L24, and R26 provide negative feedback for Q21B. The output of the driver, collectors of Q21A and Q21B, is transformer coupled by T2 to the output amplifier. The driver stage is a class AB amplifier with a gain of about 10, 1W in 10 W's out. T2 is a step-down, center-topped 2:1 turn transformer.

The output stage, common-emitter transistor Q41A and Q41B, is enabled, as explained above, during transmit operation by the +9-V xmt input at J3 pin 5 and 7. The voltage applied to voltage divider CR62, R63 and R62 is regulated at +5.1 V by VR21. Variable resistor R63 adjusts the idle current of the output amplifier. The positive dc voltage on the wiper of R63 is applied to the noninverting input of differential amplifier U101B pin 5. The positive output of U10B, pin 7, provides forward bias for Q61. With the 100 percent feedback from the emitter of Q61 to the inverting input of U101B pin 5 the voltage gain from U101B, pin 5, to the emitter of Q61 is one. Diode CR62 provides temperature compensation for the output amplifier. Variable resistor R63 is adjusted to produce an idle current of approximately 250 mA in the output amplifier. Vcc for the output amplifiers is the high current +14 V dc applied through R43 and T3 to the collectors Q41A and Q41B. The output of the output stage, taken from the collector of Q41A and Q41B is transformer coupled by T4 to rf out, P2. T4 is a step up transformer with a turns ratio of 2:5. The output power at P2 is 100 W pep nominal. In CW or RTTY operation the power is automatically turned down to 50 W after 10 seconds. The output amplifier operates class AB with a gain of approximately 10, 10 watts in, 100 watts out.

4.3.8 PA ALC and Protection Circuits

Refer to figure 4-10 in the self-study manual and the pa schematic in the service manual.

The ALC and protection circuits for the KWM-380 are located in the A1 (power amplifier) module. The forward power detector (FWD PWR DET) input at J3, pin 15, is a positive dc voltage, originating in the low-pass filter assembly A2, that is proportional to the forward power out. The input at pin 15, nominally +2 V dc with 100 watts of rf power, if applied to the noninverting input of U81A, pin 3, through low-pass filter L81 and C81. The output of U81A, pin 1, is integrated at capacitor C85 to produce a dc voltage that is proportional to the average rf output power. The voltage on C85 is applied through Q83 to the noninverting input of the ALC summing amplifier U101A, pin 3. With no inversion through U81A or Q83 the dc voltage applied to pin 3 of U101A, proportional to forward power out, is applied to the bias control circuit of the predriver Q1 and through CR103 to charge C106 and C104. The voltage at C104, J3, pin 18, is an output of A1 that is routed to the receiver/exciter board to control the exciter gain. The average power amplifier can be disabled by a logic 0 input to A1 on J3, pin 17, average ALC inhibit, (AVG ALC inhibit). By placing a logic 0 on pin 17, CR84 is forward biased, the base of Q83 is at approximately +0.5 V dc, and Q83 is reverse biased.

With the average power amplifier inhibited by a logic 0 at J3, pin 17, rf power output is controlled by the peak power amplifier U81B. The input to the peak power amplifier, noninverting input, pin 5 is the positive dc voltage from the forward power detector. The gain a U81B can be altered by a logic level change at J3, pin 8, (tune power). A logic 1 on the tune power input will cause a reduction in the peak rf output power of the pa. With a logic 1 at pin 8, diode CR85 is reverse biased, VR81 and Q81 are forward biased removing R95 from the

feedback circuit of U81B. With R95 removed from the circuit the gain of U81B is approximately 0.65. With a logic 0 on pin 8, CR85 is forward biased, VR81 and Q81 are reverse biased and transistor switch Q82 is on placing R95 and R81 in parallel. With R95 and R81 in parallel, gain of U81B is increased to approximately 3.4. Because the forward power detector input is applied to the noninverting input of U81B, the output at pin 7 is proportional to forward power. When the output of U81B, pin 7, is sufficiently positive to forward bias CR81, current flows from ground, through R108 and CR81 to U81B. The voltage developed across R108 is input to U101A pin 3. An increase is forward power out of the pa, through the peak power amplifier and the ALC summing amplifier will produce an increase in ALC voltage out at J3, pin 18.

A dc voltage, proportional to the reflected power at the output of the pa, is input to the A4 module at J3 pins 14 and 15, (REFL PWR DET). This positive dc voltage is filtered by low-pass filter L82 and C83 and applied to pin 10 of U81C. Pin 10 of U81C is the noninverting input, the output at pin 8 has a voltage gain of 4 with no phase inversion. With the output of U81C sufficiently positive to forward bias CR83, current flows from ground, through R108 and CR83 to U81C. The voltage developed across R108 is applied to the noninverting input of ALC summing amplifier U101A. In an operating condition where the reflected power increases to an unsafe level the positive input to U101A, pin 3, will cause the output, pin 1 to go more positive to reduce the gain of the exciter and pa.

The output amplifiers in the KWM-380 are protected against excessive current, >23A, by the current sensing circuit. The Vcc for transistors Q41A and Q41B is the high current, +14 V dc applied through R43, (0.01 Ω) and T3. Variable resistor R45 (in the voltage divider R46, R45, and R44) from ground to +14 V dc determines the offset voltage applied to pin 12, the noninverting input of current sense amplifier U101D. The adjustment range of R45 is approximately +2.16 V to +2.46 V dc. The voltage at the inverting input of U101D is determined by the voltage drop across current sense resistor R43. With a current of 23 A through R43, the voltage applied to pin 13 of U101D is +2.25 V dc. R45 is adjusted to give a positive output, sufficient to forward bias CR102, when the current through R43 exceeds 23 amps. With CR102 forward biased, current flows from ground, through R108 and CR102 to pin 14 of U101D. The increase in voltage, developed across R108, causes the output voltage at pin 1 of U101A to increase, reducing the power out of the exciter and pa until the current through R43 drops below 23 amps.

The KWM-380 is also protected against excessive temperature in the pa by the ALC thermal limiting circuit, the output of which is applied to the inverting input, pin 2, of ALC summing amplifier U101A. When operating at normal temperatures the biasing of U101C keeps the output, pin 8, highly positive. Zener diode VR101 regulates the voltage at the junction of R105 and R106 at +5.1 V. R106 is adjusted by inhibiting the average power amplifier, ground on J3, pin 17, driving the pa output to 100 W and adjusting R106 for +1.0 ±0.3 V out at J3 pin 18. The temperature of the pa is sensed by thermistor RT101 which is on the pa heatsink. RT101 has a negative temperature coefficient so as the temperature increases the voltage drop across RT101 decreases. With the voltage at the junction of RT101 and R101, noninverting input, pin 10 of U101C decreasing, the voltage at the output of U101C, pin 8, decreases. With increasing temperature, output voltage of U101C continues to drop. When the output drops below +5.1 V, current flow through VR101 stops and any additional decrease in voltage is sensed at R106 and applied to the inverting input of U101A, pin 2. As the voltage at pin 2 of U101A decreases, the output voltage increases to reduce the rf output power from the exciter and pa.

The transmit monitor output, J3, pin 6, and power meter output, J3, pin 16 are controlled by the output of the peak power amplifier U81B. The dc voltage, proportional to output power, is applied to pin 16, through R115 and is routed to the front panel meter. When the output

of U18B exceeds +1.8 V dc (approximately 50 watts) current through VR102 forward biases C[illegible]1 producing a logic 0 at pin 6.

4.3.9 Low-Pass Filter, T/R Relay and Directional Coupler A2

Refer to figure 4-11 in the self-study manual and the low-pass filter schematic in the KWM-380 Service Manual.

From the output of the power amplifier module, A1P2, the transmit rf signal enters the low-pass filter at A2J1. From J1 the signal is applied to pin 4 of T/R relay K1. K1 is energized in transmit by the +9-V dc xmt at J3, pin 7. With the relay energized, the rf is routed through the relay, pin 4 to pin 3, and into A2A1 at E8. At E8 the rf is applied to the inputs of the five low-pass filter sections. Only one of the low-pass filter sections is enabled at a time, determined by the operating frequency. Band information required to enable the filter is applied at A2A1J1, pins 6 through 10. With a transmit frequency between 3.500 and 4.000 MHz, a logic 0 would be applied to pin 7, from control card A8, pins 6, 8, 9, and 10 would be at logic 1. A logic 0 (ground) at pin 7 energizes K3 and K8 to allow the signal through the filter. The transmit signal is routed out of A2A1 at E9 where it re-enters A2A2. From E9 the rf passes through T1 to the antenna jack J2 on the rear of the transceiver.

T1 and the associated components make up the forward and reflected power detectors. Rf current at the output of the pa is sampled at T1, the voltage induced in the secondary of T1 is applied to the anode of CR2. Rf output voltage is sampled, through variable capacitor C1 and L2, and applied to the cathode of CR2. C2 is adjusted to give a detected, dc voltage of +2.2-V at the cathode of CR2 with 100 watts of forward power. The voltage from the detector, CR2, is filtered by low-pass filter C4, L4, and C6 and applied to J3, pin 3.

he reflected power detector the rf current is sampled by T1 and the voltage induced in the secondary is applied to the anode of detector CR1. The rf voltage, sampled through variable capacitor C1 and L1 is applied to the cathode of CR1.

C1 is adjusted to give +0.1 V dc with a standing wave ratio of 1:1 into a 50 load. The output of the detector is filtered by low-pass filter C3, L3, and C5 and applied to J3, pin 2. With 100 watts of reflected power the output at J3, pin 2, would be +2.2 V dc.

4.5 SELF-TEST

1. If A3 (L509 on the receiver-exciter board) opens, the KWM-380 will not transmit in SSB because _____.
2. With lower sideband, transmit operation, variable resistor A4R____in the passband tuning circuit determines the frequency of oscillator Q2.
3. How is the front panel control, PBT (pass band tuning) disabled during transmit operation? _____.
4. To reduce the gain of transmit if amplifier A3Q104, the voltage applied to gate 2 of Q104 must _____.
5. With a variable injection input to A3U100, pin 8 of 67.12345 MHz, the transmitter output frequency is _____MHz.
6. With 250 mA of idle current in the pa driver stage, the voltage drop across A1A1R28, TP2 to TP3 is _____mV.
7. With a logic 1 at A1A2J3, pin 8, the voltage gain of U81B is_____ _____.
8. With excessive reflected power, the output of A1A2, U101A, pin 1, will _____ _____to reduce pa output power.
9. A1A2, R45, in the current sense amplifier is adjusted to limit the pa output power when the current through R43 exceeds _____ A.
10. A2A2 (C2 in the directional coupler) is adjusted to provide a _____V output at J3 pin 3 with 100 watts of forward power.

4.6 SELF-TEST ANSWERS

1. CR502 is reverse biased, blocking the 455-kHz input to the modulator.

2. R34

3. A logic 0, or ground, applied to J1, pin 16 of the passband tuning circuit keeps switch U1D open to disable PBT during transmit operation.

4. Decrease

5. 27.97845 MHz

6. +27.5 mV

7. +0.65

8. Increase

9. 23A

10. +2.2 V dc

5.1 OBJECTIVES

5.2 BLOCK DIAGRAM ANALYSIS

5.2.1 Principles of Phase-Locked Loops

Figure 5-1

5.2.2 Block Diagram Analysis of KWM-380 Synthesizer

Figure 5-2

5.3 SYNTHESIZER SCHEMATIC ANALYSIS

5.3.1 Loop 1

Figure 5-3

5.3.2 Loop 2

Figure 5-4
Figure 5-5
Figure 5-6

5.3.3 Variable Reference Frequency Loop

Figure 5-7
Figure 5-8
Figure 5-9
Figure 5-10
Figure 5-11
Figure 5-12

5.4 OSCILLATOR ASSEMBLY A7 ANALYSIS

5.5 SELF-TEST

5.6 SELF-TEST ANSWERS

5.1 OBJECTIVES

In this section the student will become familiar with the operation of the frequency synthesizer and the oscillator assembly. At the conclusion of this section the student should be able to accomplish the following:

a. Understand the principles of phase locked loop synthesizers.
b. Identify the three loops in the synthesizer.
c. Know the interaction between loops in the synthesizer.
d. Know the frequency control input to the synthesizer for any operating frequency.
e. Be able to determine the variable injection output frequency for any operating frequency.
f. Know the count sequence of both variable dividers.
g. Understand the operation of the oscillators in the oscillator assembly.

5.2 BLOCK DIAGRAM ANALYSIS

5.2.1 Principles of Phase-Locked Loops

Refer to figure 5-1. A phase-locked loop (PLL) compares the frequency and phase of its voltage-controlled oscillator (VCO) output to that of a reference frequency. If the two signals differ in frequency or phase, an error voltage is developed and applied to the VCO. This causes the error voltage to shift the VCO frequency in the direction necessary to decrease the difference. Frequency correction continues until lock is achieved, after which the VCO will track the reference frequency.

Placing a programmable divider in the feedback path from the VCO to the frequency phase detector (comparator) allows the VCO output to be changed in multiples of the reference frequency. The loop output frequency then becomes some multiple, N, of the reference frequency (F out = N X F ref, where N is the division ratio of the programmable divider). Changes in the operating frequency are made by changing the driver ratio.

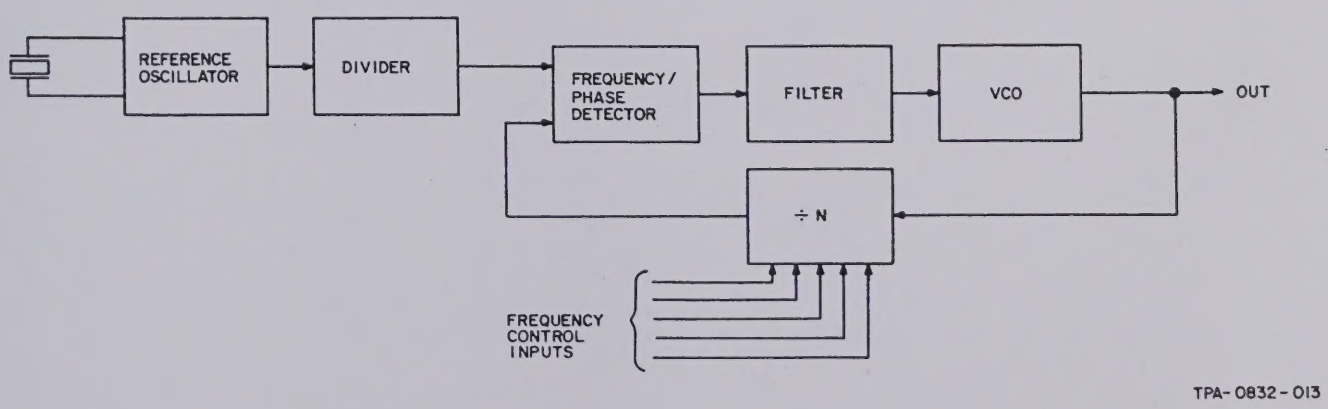


Figure 5-1. Basic Phase-Locked Loop Block Diagram.

5.2.2 Block Diagram Analysis of the KWM-380 Synthesizer

Refer to figure 5-2. The synthesizer in the KWM-380 is made up of three phase-locked loops; loop 1, or the output loop; loop 2, or the translator loop; and the variable reference frequency loop. The VCO in loop 1 is used to generate the variable injection output which has a range of 39.645 MHz - 69.14999 MHz. The minimum frequency change possible at this point is 10 Hz. The loop 1 VCO output is mixed with the loop 2 output to produce a 2.945- to 3.94499- MHz signal which is applied to a fixed $\div 10$ circuit. The output of the $\div 10$ circuit, 0.2945 to 0.394499 MHz, is compared with the output of the variable reference frequency loop in the frequency/phase detector. This second input to the loop 1 phase detector is also a 0.2945 to 0.34499- MHz signal.

The output of the loop 2 VCO, in addition to being applied to the loop 1 mixer, is applied to a variable divider. The division ratio of this divider is determined by the 1- and 10-MHz frequency information selected on the front panel. With loop 2 in a locked condition (normal operation), the output of the variable divider will be a 100-kHz signal applied to the loop 2 frequency/phase detector. The second input to this phase detector is a 100-kHz reference signal developed from the frequency standard in the oscillator A7 assembly. Changing the division ratio of the loop 2 variable divider by 10 will produce a 1-MHz change in the VCO output frequency.

The output of the variable reference frequency loop VCO is a 147.25- to 197.2495-MHz signal that is applied directly to the variable divider and through a fixed divide by 50 and divide by 10 to the loop 1 phase detector. The division ratio of the variable reference frequency loop divider is determined by the 100-kHz, 10-kHz, 1-kHz, 100-Hz and 10-Hz dial frequency. During normal operation (synthesizer locked), the output of the variable divider is a 500-Hz signal, applied to the frequency/phase detector. The second input to this phase detector is a 500-Hz signal developed from the frequency standard in A7.

A 10-Hz change in the dial frequency changes the division ratio of the variable divider by one, which produces a 500-Hz frequency change at the output of the VCO. This frequency change will be 10 Hz at the output of the divider by fifty circuit, 500 Hz $\div 50 = 10$ Hz, and 1 Hz at the input to the loop 1 phase detector, 10 Hz $\div 10 = 1$ Hz. A 1-Hz frequency change at the loop 1 phase detector reference input will produce a 10-Hz change in the variable injection output of the synthesizer.

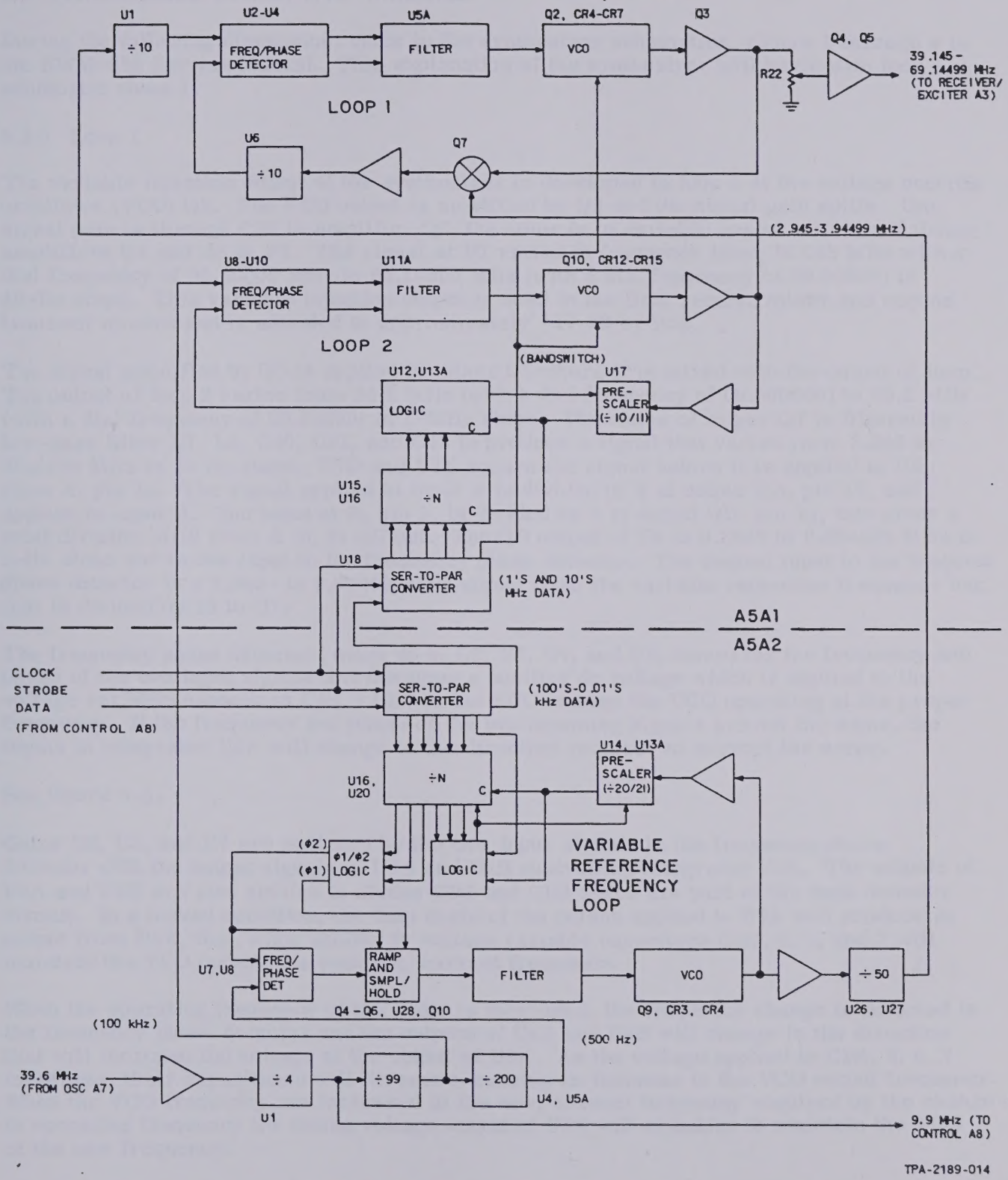


Figure 5-2. Synthesizer Block Diagram.

5.3 SYNTHESIZER SCHEMATIC ANALYSIS

During the following discussion, refer to the synthesizer schematics, sheets 1 through 4 in the KWM-380 Service Manual. This explanation of the synthesizer will begin with loop 1, schematic sheet 1.

5.3.1 Loop 1

The variable injection output of the synthesizer is developed in loop 1 at the voltage controlled oscillator (VCO) Q2. The VCO output is amplified by Q3 and the signal path splits. One signal path is through C32 to amplifier Q6, the other is to variable resistor R22, and through amplifiers Q4 and Q5 to P1. The signal at P1 varies in frequency from 39.645 MHz with a dial frequency of 00.50000 MHz to 69.14999 MHz (with a dial frequency of 29.99999) in 10-Hz steps. This variable injection output is used in the first receive mixer and second transmit mixers and is adjusted to approximately +17 dB by R22.

The signal amplified by Q6 is applied to mixer Q7 where it is mixed with the output of loop 2. The output of loop 2 varies from 36.2 MHz (with a dial frequency of 00.500000) to 65.2 MHz (with a dial frequency of 29.99999) in 1-MHz steps. The output of mixer Q7 is filtered by low-pass filter L7, L8, C40, C41, and C42 to produce a signal that varies from 2.945 to 39.4499 MHz in 10 Hz steps. U7D and U7F square the signal before it is applied to U6, input A, pin 14. The signal applied to input A is divided by 2 at output QA, pin 12, and applied to input B. The input at B, pin 1, is divided by 5 at output QD, pin 11, this gives a total division of 10 from A in, to QD out. The QD output of U6 is 0.2945 to 0.394499 MHz in 1-Hz steps and is one input to the frequency phase detector. The second input to the frequency phase detector is a 2.945- to 3.94499-MHz signal from the variable reference frequency loop that is divided by 10 in U1.

The frequency phase detector, made up of U2, U3, U4, and U5, compares the frequency and phase of the two input signals and develops a positive dc voltage which is applied to the voltage variable capacitors CR4 - CR7 in the VCO to keep the VCO operating at the proper frequency. If the frequency and phase of the two incoming signals are not the same, the inputs to integrator U5A will change in the direction required to correct the error.

See figure 5-3.

Gates U2, U3, and U4 are switched by the two input signals to the frequency phase detector with the output signals of U4A and U4B controlling integrator U5A. The outputs of U4A and U4B are also applied to diodes CR1 and CR2 which are part of the fault detector circuit. In a locked condition, the duty cycle of the pulses applied to U5A will produce an output from U5A, that, when applied to voltage variable capacitors CR4, 5, 6, and 7 will maintain the VCO output at a constant, correct frequency.

When the operating frequency of the radio is increased, the frequency change is detected in the frequency phase detector and the outputs of U4A and U4B will change in the direction that will increase the voltage at the output of U5A. As the voltage applied to CR4, 5, 6, 7 increases, their capacitance will decrease, causing an increase in the VCO output frequency. When the VCO frequency has increased to the new, correct frequency required by the change in operating frequency the tuning voltage output of U5A will stabalize to maintain the VCO at the new frequency.

If the operating frequency is lowered the above sequence would be reversed to reduce the tuning voltage applied to the voltage variable capacitors and lower the VCO frequency.

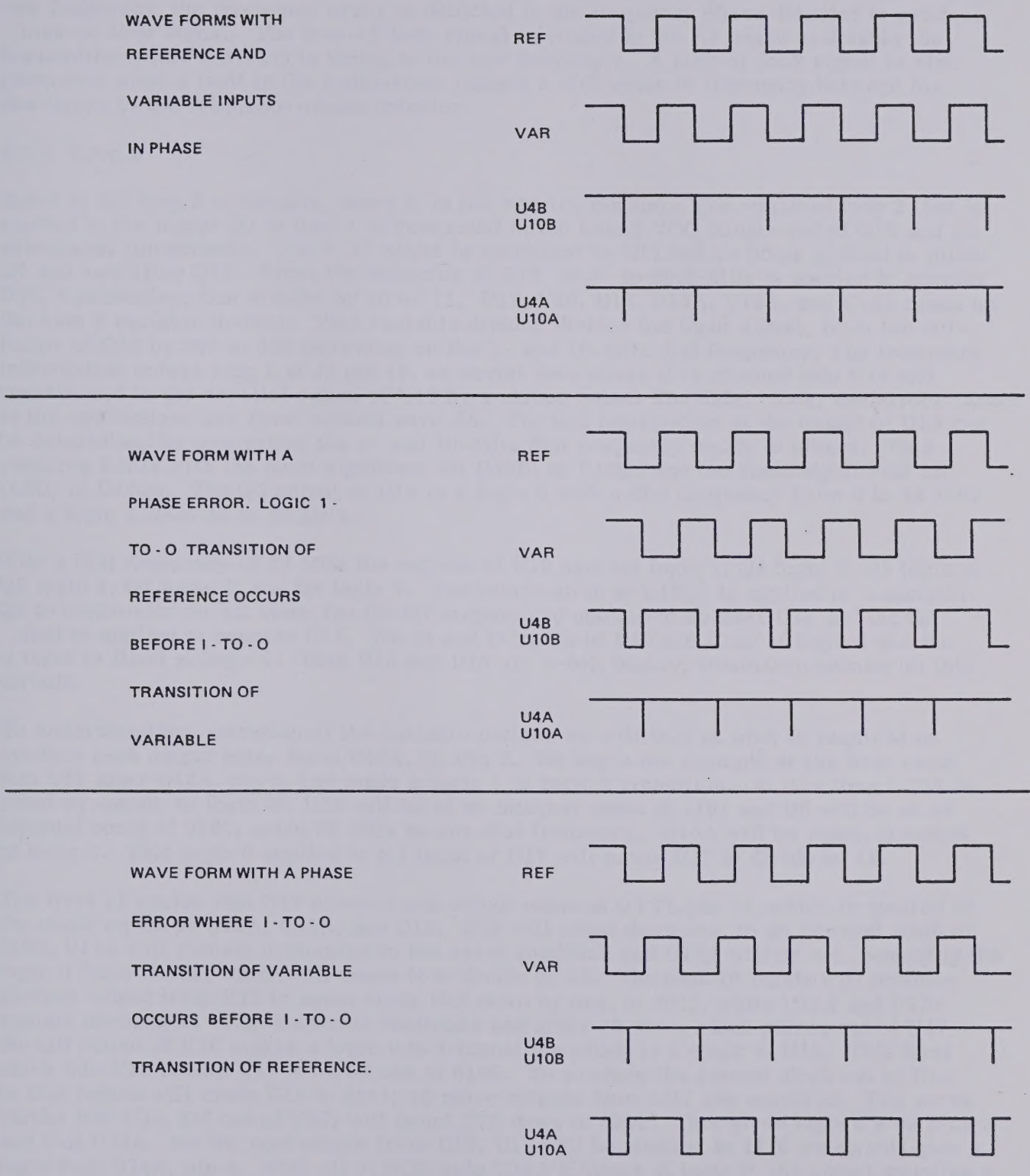


Figure 5-3. Loop 1 and 2 Frequency - Phase Detector Waveforms.

During the time between a front panel frequency change and the synthesizer locked to the new frequency, the frequency error is detected in the frequency phase detector to produce a loss-of-lock signal. The loss-of-lock signal is routed to the A3 board to disable the transmitter while the VCO is tuning to the new frequency. A loss-of-lock signal is also generated when a fault in the synthesizer causes a difference in frequency between the two inputs to the frequency-phase detector.

5.3.2 Loop 2

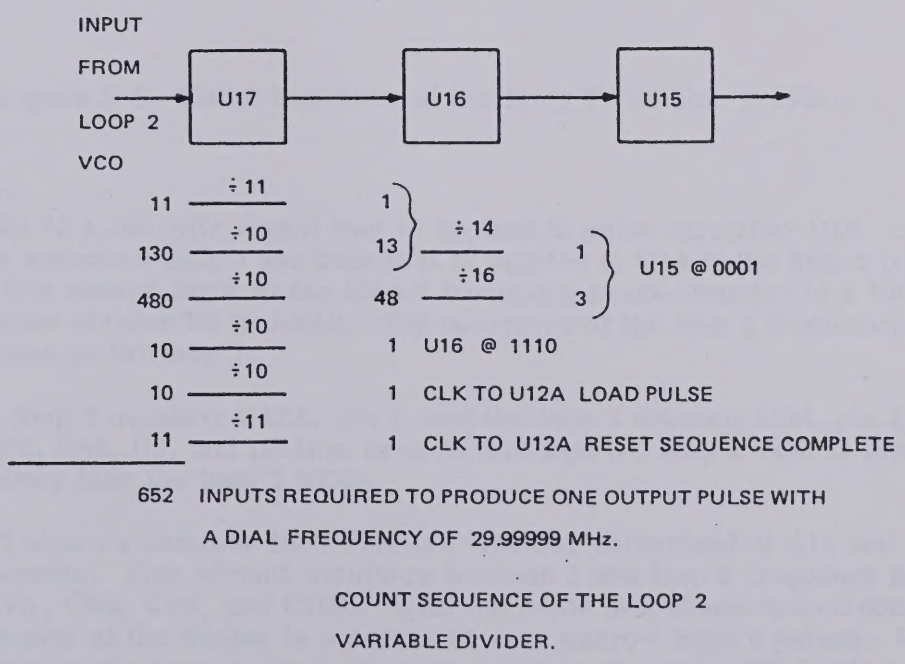
Refer to the loop 2 schematic, sheet 2, in the service manual. The output of loop 2 that is applied to the mixer Q7 in loop 1 is generated in the loop 2 VCO comprised of Q10 and its associated components. The VCO output is amplified by Q11 before being applied to mixer Q7 and amplifier Q12. From the collector of Q12 36.2-- to 65.2-MHz is applied to counter U17, a prescaler, that divides by 10 or 11. U17, U16, U15, U13A, U12A, and U14A make up the loop 2 variable divider. This variable divider divides the input signal, from the collector of Q12 by 362 to 652 depending on the 1- and 10-MHz dial frequency. The frequency information enters loop 2 at J1 pin 10, as serial data where it is clocked into U18 and transferred to the parallel output of U18 by a strobe pulse. The data, clock, and strobe inputs to the synthesizer are from control card A8. The bcd information at the output of U18 can be determined by converting the 1- and 10-MHz dial frequency (0-29) to binary. This requires 5 bits with the most signficant bit (MSB) at U18Q8 and the least significant bit (LSB) at U18Q4. The Q3 output of U18 is a logic 0 with a dial frequency from 0 to 12 MHz and a logic 1 from 13 to 29 MHz.

With a dial frequency of 29 MHz the outputs of U18 are; Q3 logic 1; Q4 logic 1; Q5 logic 0; Q6 logic 1; Q7 logic 1, and Q8 logic 1. The information at U18Q3 is applied to transistor Q9 to control its on/off state, the Q4-Q7 outputs are applied to counter U16 and the Q8 output is applied to counter U15. The B and D inputs of U15 are fixed at logic 0 and the C input is fixed at logic 1. Both U15 and U16 are 4-bit, binary, countdown counter in this circuit.

To understand the operation of the variable divider we will look at what is required to produce each output pulse from U12A, Q, Pin 5. We begin the example at the first clock into U17 after U12A, pin 5, has made a logic 1 to logic 0 transition. At this time U12A is reset (Q output to logic 0), U16 will be at an internal count of 1101 and U5 will be at an internal count of 0101, using 29 MHz as our dial frequency. U13A will be reset, Q output at logic 0. This logic 0 applied to M1 input of U17 will cause U17 to divide by 11.

The first 11 cycles into U17 produce one output pulse at QTTL pin 11, which is applied to the clock inputs of U12A, U13A, and U16. U16 will count down one, to an internal state of 1100, U12A will remain unchanged in the reset condition and U13A will be set, removing the logic 0 from U17M1 which will cause it to divide by 10. The next 10 inputs will produce another output from U17 to again clock U16 down by one, to 1011, while U12A and U13A remain unchanged. This sequence continues and after 12 more clock pulses out of U17 the QD output of U16 makes a logic 0 to 1 transition which is a clock to U15. This first clock into U15 counts U15 down by one to 0100. To produce the second clock out of U16 to U15 (which will clock U15 to 0011) 16 more outputs from U17 are required. Two more clocks into U15, (32 out of U17) will count U15 down to 0001. This gives logic 0's on pins 3 and 5 of U14A. On the next output from U17, U16 will be clocked to 1110 which will give a logic 0 on U14A, pin 4. With all of NOR gate U14A's inputs at logic 0, the output supplies a logic 1 to the D input of U12A.

With the next output of U17, U12A will be clocked to the set condition. The logic 0 at U12A $\overline{Q}$ is applied to the reset input of U13A, causing it to reset and force U17 to divide by 11 on the next count, and to the L (load) inputs of U15 and U16, forcing U15 to the internal state of 0101 and U16 to 1101. As long as the load input remains logic 0, the counter will remain in this state. When U15 and U16 are loaded, the logic 0's are removed from U14A and U12A D input is a logic 0. To produce the next output (which will reset U12A and complete one count cycle) 11 more inputs are required to U17. If we count the number of inputs to U17 required to produce one output from U12A, with a dial frequency of 29 MHz, we have 652 which is the division ratio of the counter. Another way to determine the division ratio of the loop 2 variable divider is to multiply the 1- and 10-MHz dial frequency by 10 and add it to 362. (29 X 10) + 362 = 652. Figure 5-4 shows the count sequence of the loop 2 variable divider required to produce each output pulse with a dial frequency of 29 MHz. Figure 5-5 shows the count sequence with a dial frequency of 00.99999 MHz. Figure 5-6 shows the internal count sequence and the output state of the loop 2 counter.



COUNT SEQUENCE OF THE LOOP 2 VARIABLE DIVIDER.

Figure 5-4. Count Sequence of the Loop 2 Variable Divider.

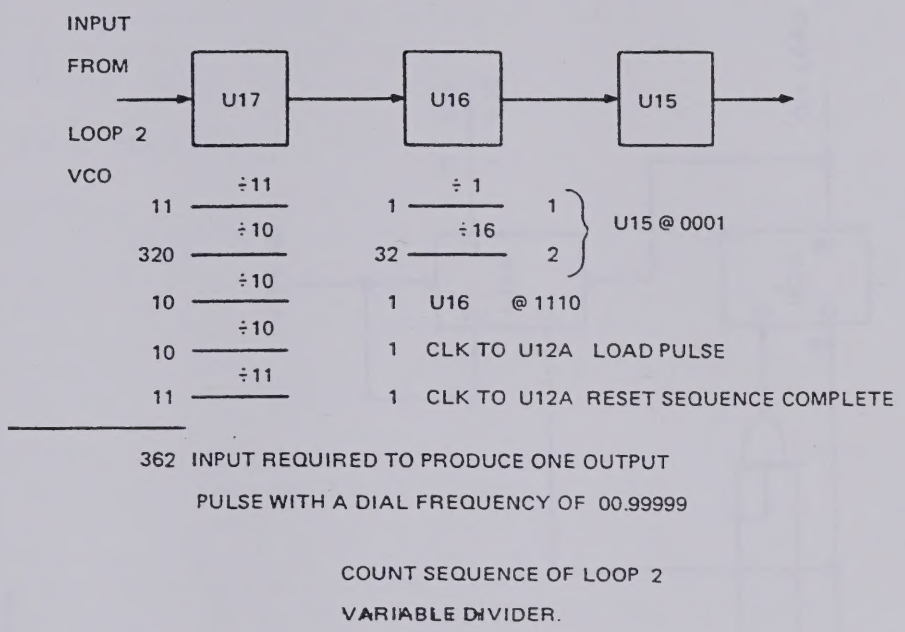


Figure 5-5. Count Sequence of the Loop 2 Variable Divider.

The output of U12A is a 100-kHz signal that is applied to pulse stretcher U12. U12 increases the pulse width to approximately 1 ms before it is applied to Q14 in the loop 2 frequency phase detector. The second input to the loop 2 frequency phase detector is a 100-kHz signal from the fixed divider U3 in A5A2. The operation of the loop 2 frequency phase detector is the same as for loop 1.

The output of the loop 2 detector U11A, pin 1, and the loop 1 detector U5A, pin 1, are connected through R61, R88, R9, and R8 this is to ensure that the loop 2 VCO is always operating at a higher frequency than the loop 1 VCO.

Loop 1 and loop 2 share a common lock monitor detector comprised of Q15 and Q16 and their associated components. This circuit monitors the loop 1 and loop 2 frequency phase detectors through diodes CR1, CR2, CR9, and CR10. With the loops in a phase-locked condition, the signal on the cathodes of the diodes is a series of very narrow logic 0 pulses. With the diodes conducting only during the logic 0 pulse, capacitor C48 is charged sufficiently to keep Q16 cut off. With Q16 cut off, Q16 is reversed biased, and a logic 1 is present at J1, pin 9. A logic 1 at pin 9 indicates that both loop 1 and loop 2 are operating in a locked condition.

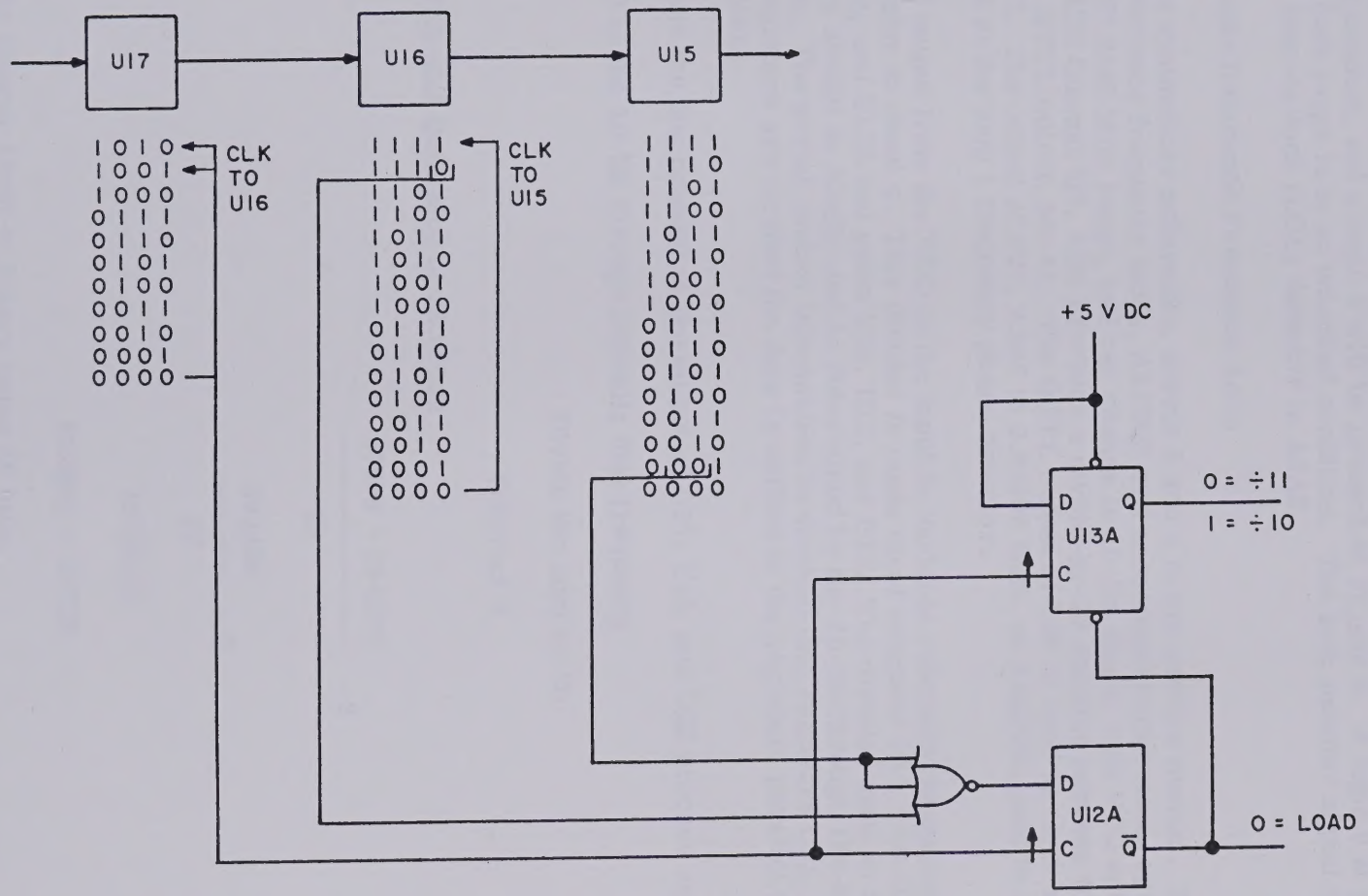


Figure 5-6. Internal Count Sequence and Output of the Loop 2 Divider.

If the two input signals to either frequency phase detector are not the same frequency and phase the width of the logic 0 pulse applies to the diodes will increase. See figure 5-7. the logic 0 pulse width increases to a duty cycle of approximately 15 percent (1.5 μs), 48 will discharge sufficiently for Q16 to conduct. When Q16 conducts, Q15 is forward biased, will conduct, and a logic 0 will be present at J1, pin 9. A logic 0 at pin 9 indicates that one or both loops is in an unlocked condition. The lock monitor signal at J1, pin 9, goes to the loss-of-lock (LOL) detector in A5A2.

5.3.3 Variable Reference Frequency Loop

Refer to the synthesizer schematic, sheets 3 and 4 in the service manual. The VCO in the variable reference frequency loops, A5A2Q9 and associated components, operates from 147.25 to 197.2495 MHz range, and can change in 10-Hz steps. One VCO output is applied to counter U26 through Q7. U26 provides a divide-by-10 function between the clock input, pin 16, and QTTL output, pin 11. The QTTL output of U26 is used to clock a divide-by-5 counter U27. The output of U27, 2.945 to 3.94499 MHz, at A5A2P6, goes to A5A1J2 where it is one input to the loop 1 frequency phase detector.

The second output from the VCO is the input to variable reference frequency loop variable divider. Refer to sheet 4. This divider is made up of counters U14, U16-U20, flip-flops U12A, U13A, and U13B and gates U10, U11, and U15. The division ratio of this divider varies from 294500 to 394499 and is determined by the 10-Hz through 100-kHz dial frequency information. The serial control information is clocked into registers U21, U22, and U23 and when the registers are strobed the data is shifted to the registers parallel outputs to be used by the counters.

To determine the bcd present at the output of U21, U22, and U23 proceed as follows:

d 294500 to the 10-Hz through 100-kHz dial frequency

Divide the sum by 20

Subtract 2

Example with dial frequency of 29.99999

$$\frac{99999 + 294500}{20} - 2$$

$$\frac{394499}{20} - 2$$

19722.95

Integer = 19722

Convert the integer 19722 to binary using 16 bits.

MSB 0100 1101 0000 1010 LSB

These 16 bits will be available to the counters U17 through U20. The most significant bit at 0D, pin 9, and the least significant bit at U17A, pin 15.

The five data bits present at the parallel outputs of U23Q4 through Q8 can be determined as follows.

$$\text{Previous division} = \frac{394499}{20}$$

Integer of division = 19724

Remainder of division 0.95

0.95 X division (20) = 19

Convert 19 to binary using 5 bits - 10011

MSB 10011 LSB

These five bits will be at U23Q4 through Q8 with the most significant bit at Q8 and the least significant bit at Q4.

To understand the count sequence we will look at what is required to produce one output pulse from the entire variable divider. Our starting point will be the first input to the divider after the load line, U12A, pin 6, makes a logic 0 to 1 transition.

With a dial frequency of 29.99999, the counters and flip-flops will be in the following states at the beginning of the count sequence.

U16 at an internal state of 0011

U17 at an internal state of 1010

U18 at an internal state of 0000

U19 at an internal state of 1101

U20 at an internal state of 0100

U13B set

U12A Reset

U14 and U13A, a divide-by-20 or 21 prescaler is set to divide by 21 with both M1 and M2 inputs to U14 and logic 0. U16, U15, and U13 determine the number of times the prescaler will divide by 21 in each count sequence.

At the beginning of this count sequence the first 21 inputs to U14 from Q8 will produce a logic 0 to logic 1 transition at U13A, pin 5, this is a clock to U16, U17, and U12A. U16 will count down one to 0010, U17 will count down to 1001 and U12A will remain unchanged in the reset condition.

With the prescaler dividing by 21, 63 more inputs to the prescaler will produce 3 more clock pulses to U16 and U17. This will clock U16 to 1111 and the 0 to 1 transition at U16QD will clock U13B to the reset condition. U17 will be clocked to 0110.

147 additional input will count U16 to 1000 and U17 to 1111. The 1 to 0 transition of U17QD is the first clock pulse to U18 and it will be clocked from 0000 to 1111. The logic 0 to 1 transition of U18QD will clock U19 to 1100.

With eight more output from the prescaler while dividing by 21, U16 is clocked to 0000. At this time the minimum/maximum output (MM), pin 12, makes a logic 0 to 1 transition. This makes both inputs to NAND gate U15C logic 1, the output of U15C is logic 0, U15B, pin 5, is logic 0, U15B output, pin 6, is logic 1. This logic 1 is applied to the enable (E) input of U16 to disable the counter and it is applied to U14, MI, pin 2, to make the prescaler divide by 20.

To reach this point in the count sequence the prescaler has divided by 21, nineteen times which is the binary number present at U23, Q4 through Q8. From this time until another load pulse is generated the prescaler will divide by 20.

A total of 312599 inputs are required to count U20 down to 0000 and develop a logic 1 on the MM output to NAND gate U11C.

40960 additional inputs will count U18 to 1011. At this time all inputs to U10B are at logic 0 and the output of U10B, Ø1, goes to logic 1.

With 20480 more inputs, U19 is at 0011 which causes the output of U10B, Ø1, to go to logic 0, and the output of U10A, Ø2, to go to logic 1.

15360 additional inputs count U19 to 0000 and develops a logic 1 out of NAND gate U11C. 4800 additional inputs count U18 to 0000. 300 additional inputs count U17 to 0000.

At this time NOR gate U10C has logic 0's on all inputs and a logic one output to U12A, pin 2. With 20 more inputs to U14, U12A will be clocked to the set condition. With U12A set (U12A $\overline{Q}$, which is the load line) is at logic 0. At this time U16 through U20 are forced to the internal state at the start of this example.

When the counters are loaded the output of U10A, Ø2, makes a logic 1 to 0 transition.

To complete the count sequence one more clock pulse to U12A is required. With the prescaler still dividing by 20, 20 additional inputs will produce one clock to U12A, U12A will reset and the count sequence is complete. Figure 5-7 shows the count sequence of the variable reference frequency loop variable divider required to produce each count sequence with a dial frequency of 29.99999 MHz. Figure 5-8 shows the same sequence with a dial frequency of 29.00000 MHz.

If the inputs required to produce one count cycle for a dial frequency of 29.99999 MHz are added up, we find 394499. 394499 inputs for one output or a division ratio of 394499. The division ratio of this loop can also be calculated by adding the 10-Hz through 100-kHz dial frequency to 294500. 294500 + 99999 = 394499. Figure 5-9 shows the internal count sequence and output states of the counter.

The Ø1 and Ø2 outputs from the variable divider are used in the reference frequency loop frequency phase detector and sample and hold circuit. Refer to schematic, sheet 3. While the variable divider is counting down, C27 is charging through constant current source Q6. When the Ø1 output of the divider goes to a logic 1, switches U28A, U28B, and U28D close, transferring the charge on C27 to C54. When Ø1 reverts to a logic 0, C54 is isolated from C27, however, at the same time Ø2 makes a logic 0 to 1 transition which closes switch U28C, transferring the charge on C54 to C57. See figures 5-10, 5-11, and 5-12.

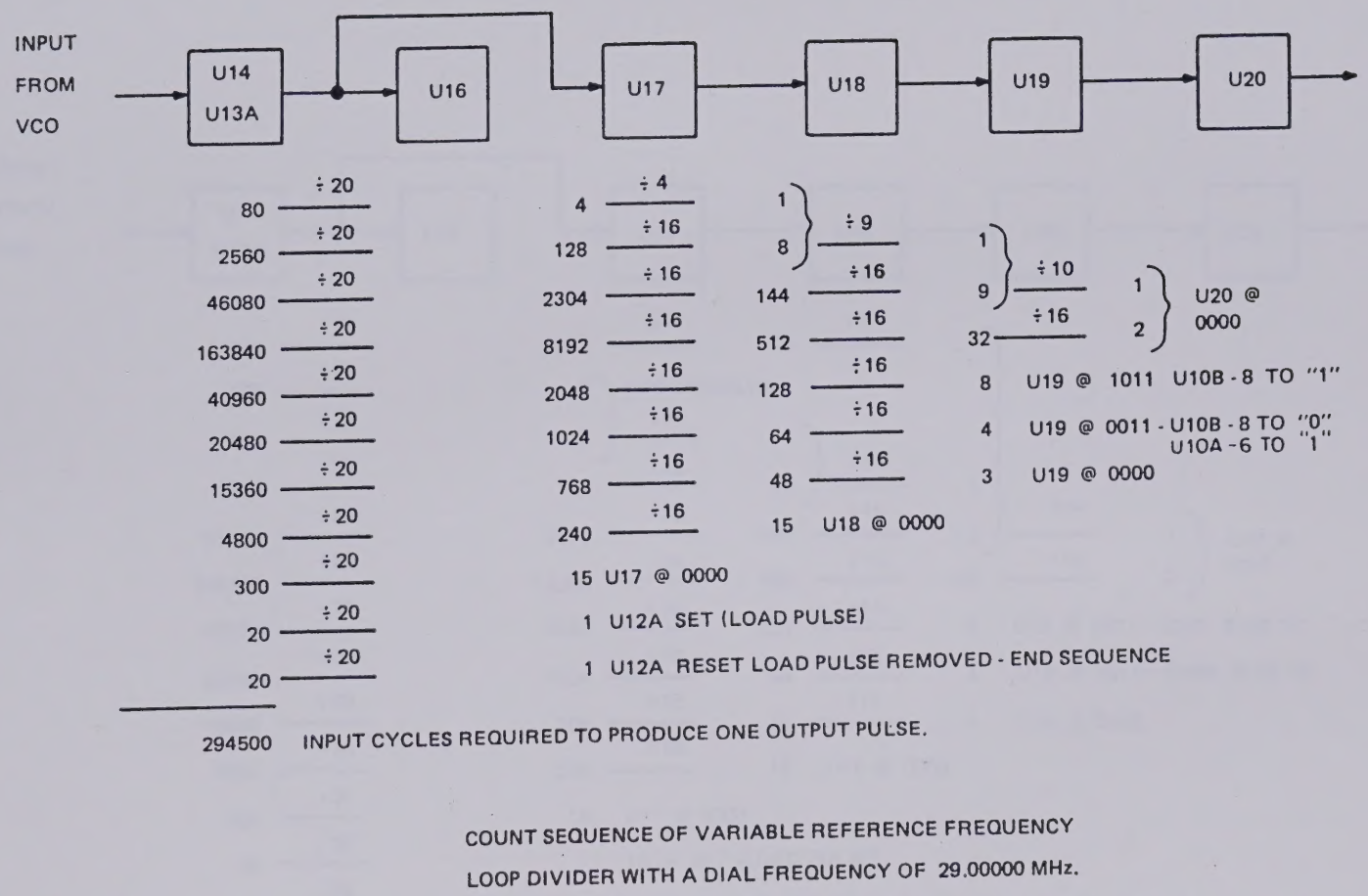
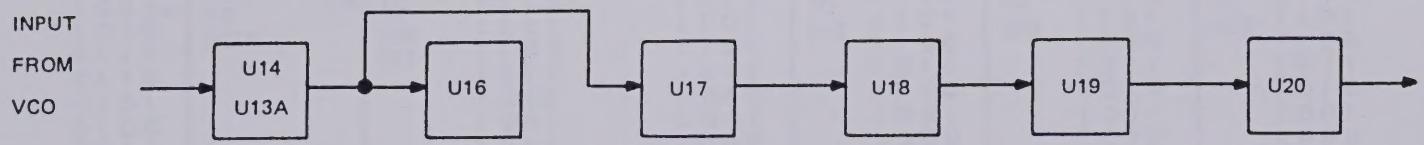


Figure 5-7. Count Sequence of the Variable Frequency Loop Variable Divider.



231	÷21	
168	÷21	
160	÷20	
4800	÷20	
61440	÷20	
245760	÷20	
40960	÷20	
20480	÷20	
15360	÷20	
4800	÷20	
300	÷20	
20	÷20	
20	÷20	
11	÷11	
8	U16 DISABLED	
8	÷16	
240	÷16	
3072	÷16	
12288	÷16	
2048	÷16	
1024	÷16	
768	÷16	
240	÷16	
15	U17 @ 0000	
1	U12A SET (LOAD PULSE)	
1	U12A RESET LOAD PULSE REMOVED - END SEQUENCE	
1	÷1	
1		
15	÷16	
1		
192	÷16	
768	÷16	
128	÷16	
64	÷16	
48	÷16	
15	U18 @ 0000	
1		
12	÷14	
48	÷16	
1	U20 @ 0000	
3		
8	U19 @ 1011 - U10B - 8 TO "1"	
4	U19 @ 0011 = U10B - 8 TO "0"	
3	U19 @ 0000	
394499	INPUT CYCLES TO PRODUCE ONE OUTPUT PULSE.	

COUNT SEQUENCE OF VARIABLE REFERENCE FREQUENCY
LOOP DIVIDER WITH A DIAL FREQUENCY OF 29.99999 MHz.

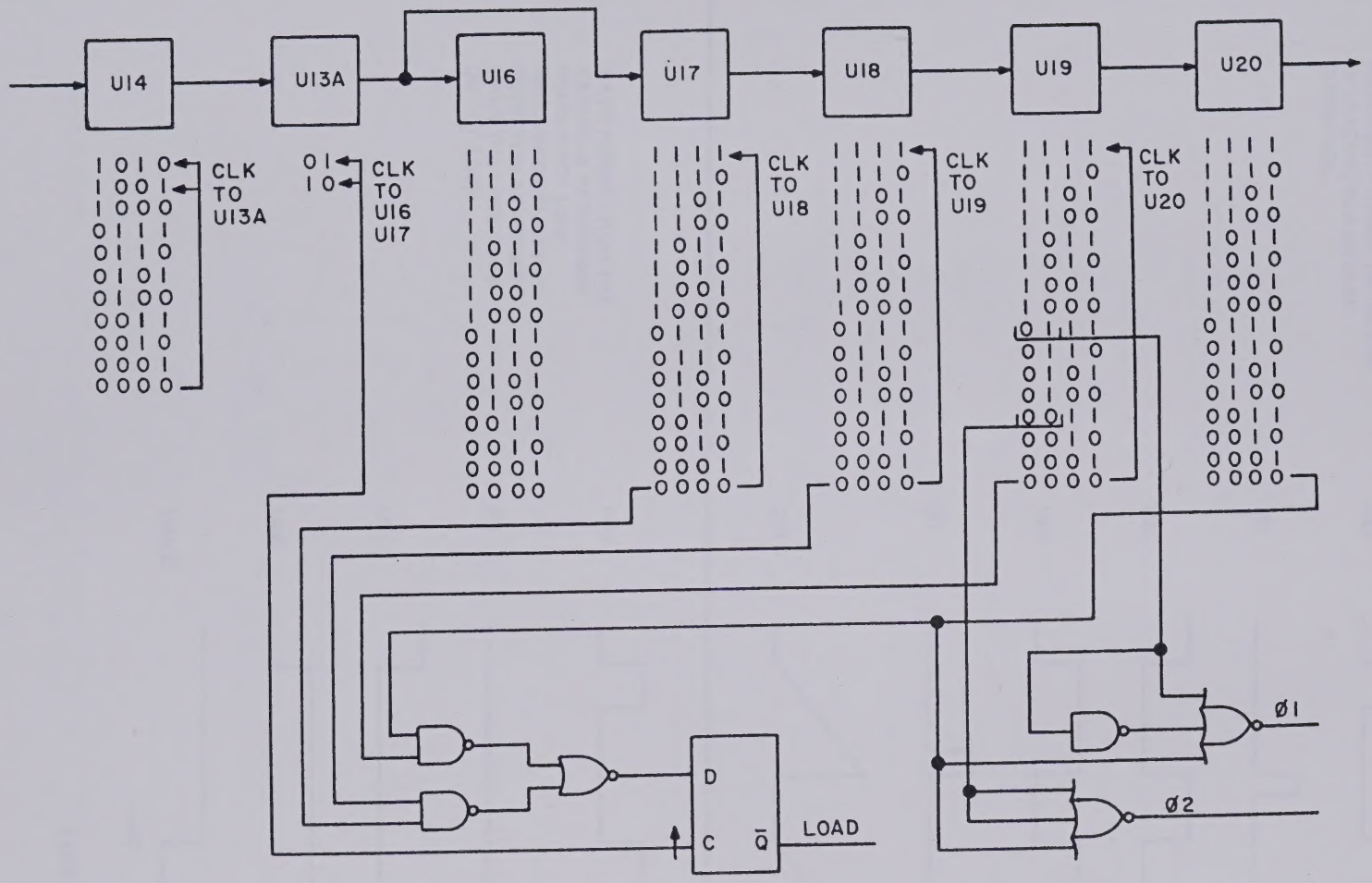
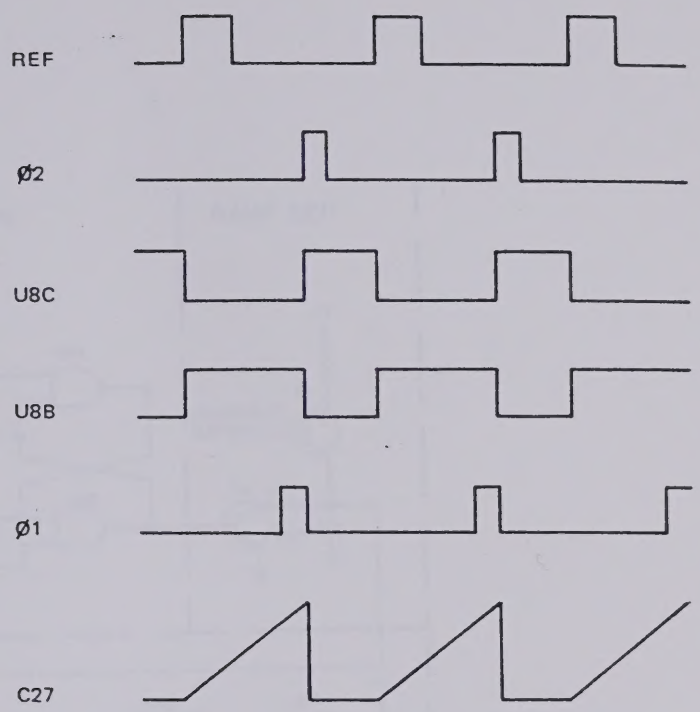


Figure 5-9. Internal Count Sequence and Output of the Variable Reference Loop Variable Divider.

WAVE FORMS FOR VARIABLE REFERENCE FREQUENCY LOOP, FREQUENCY/PHASE DETECTOR OPERATING IN A LOCKED CONDITION.



WAVE FORMS FROM THE VARIABLE REFERENCE FREQUENCY LOOP, FREQUENCY/PHASE DETECTOR AT A TIME WHEN THE LOOP GOES OUT OF LOCK.

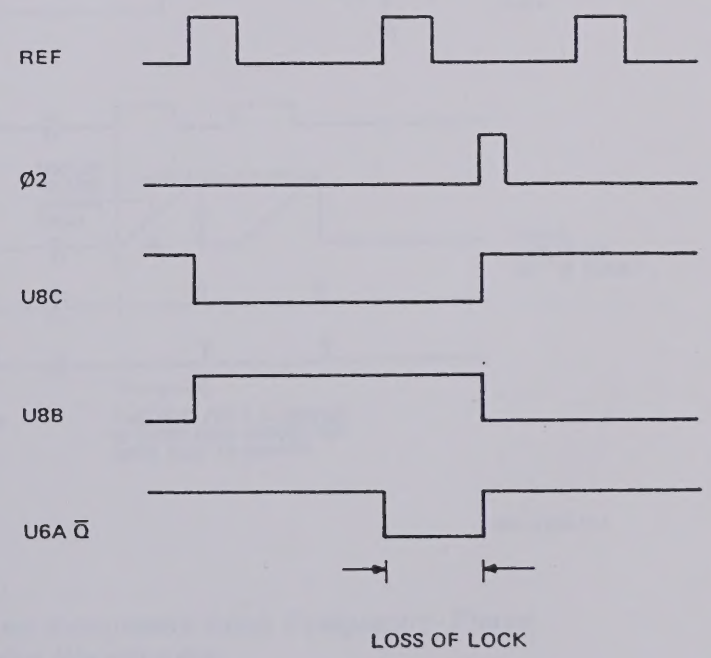


Figure 5-10. Variable Reference Frequency Loop Frequency-Phase Detector Waveforms.

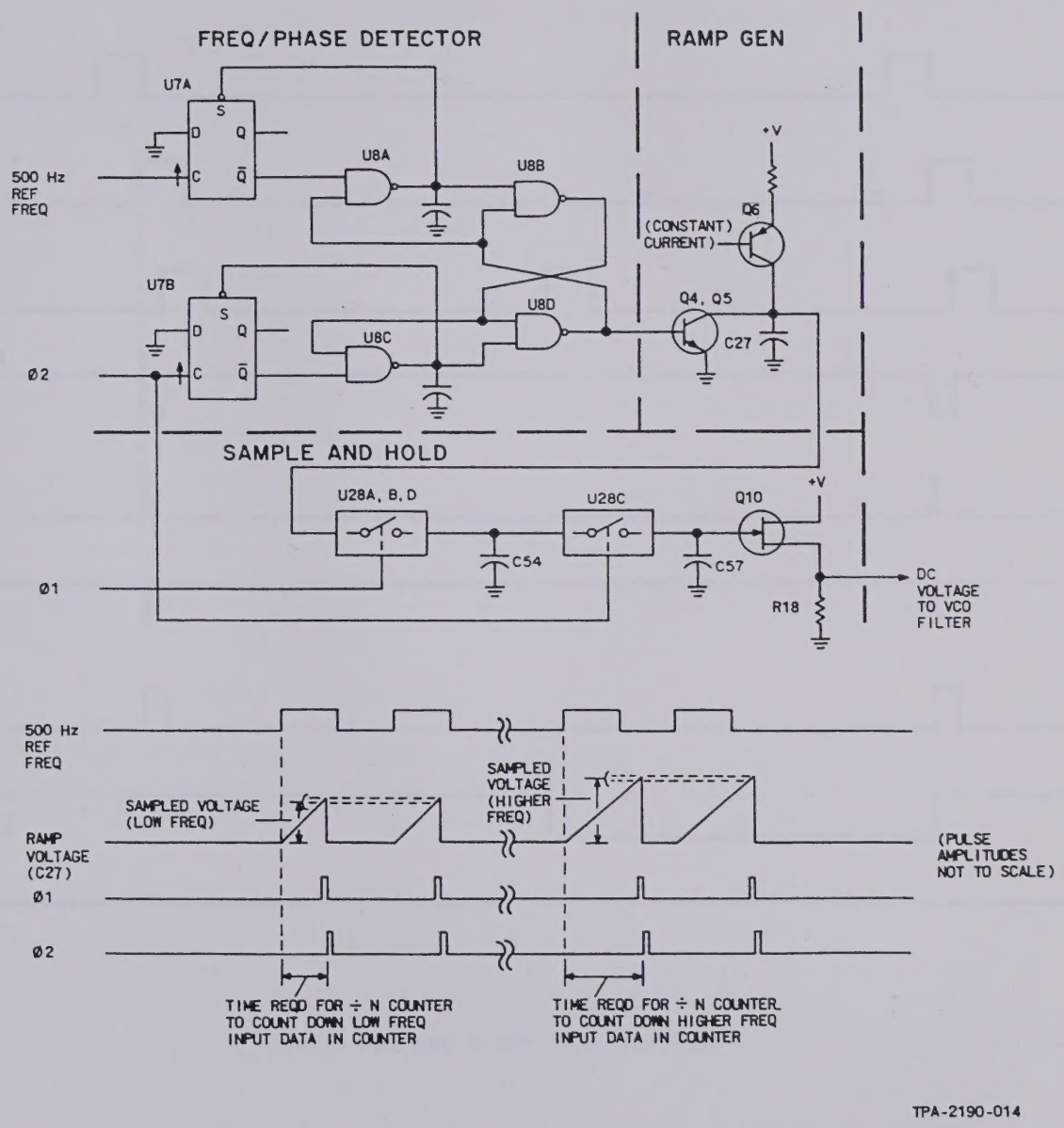


Figure 5-11. Variable Reference Frequency Loop Frequency-Phase Detector Waveforms.

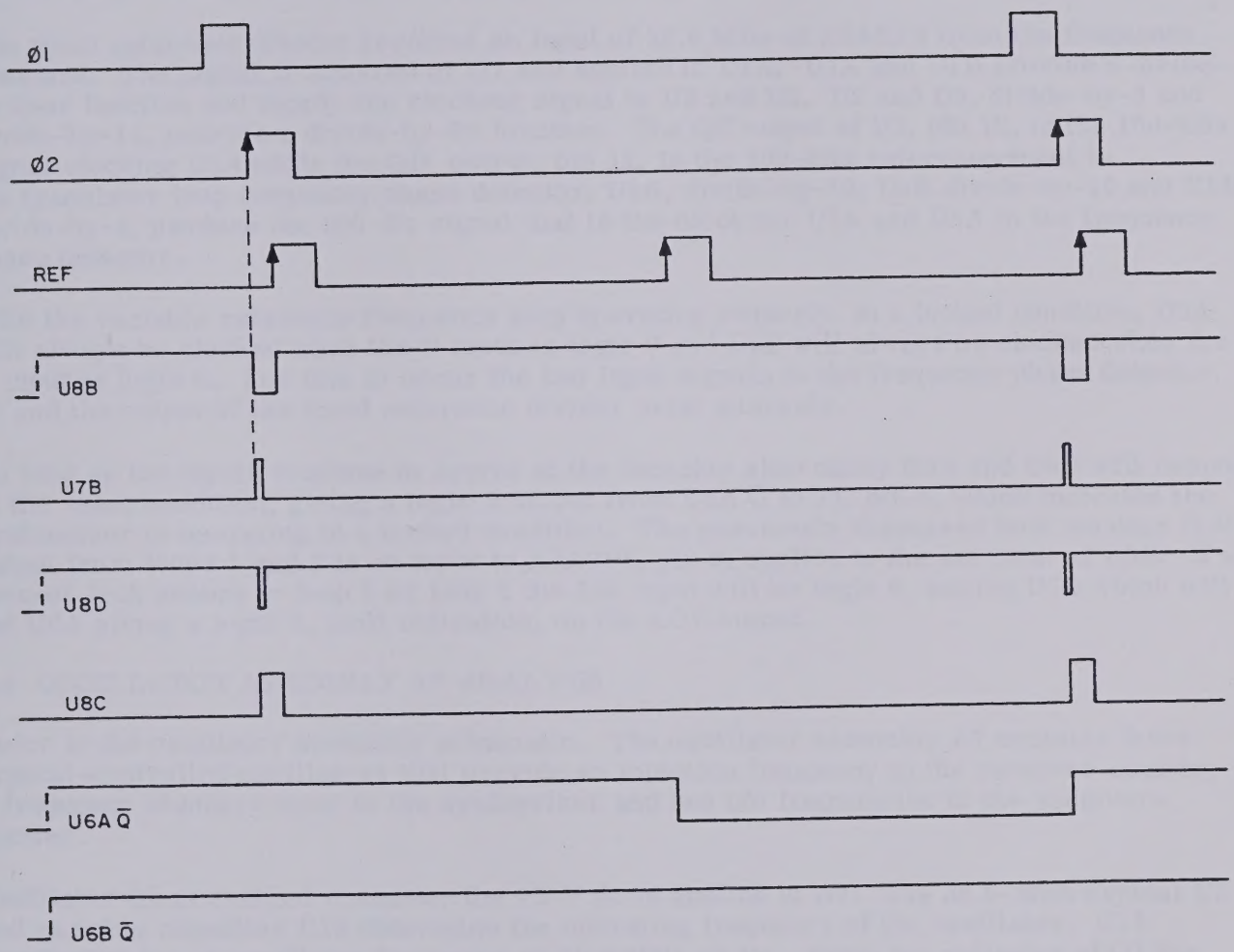
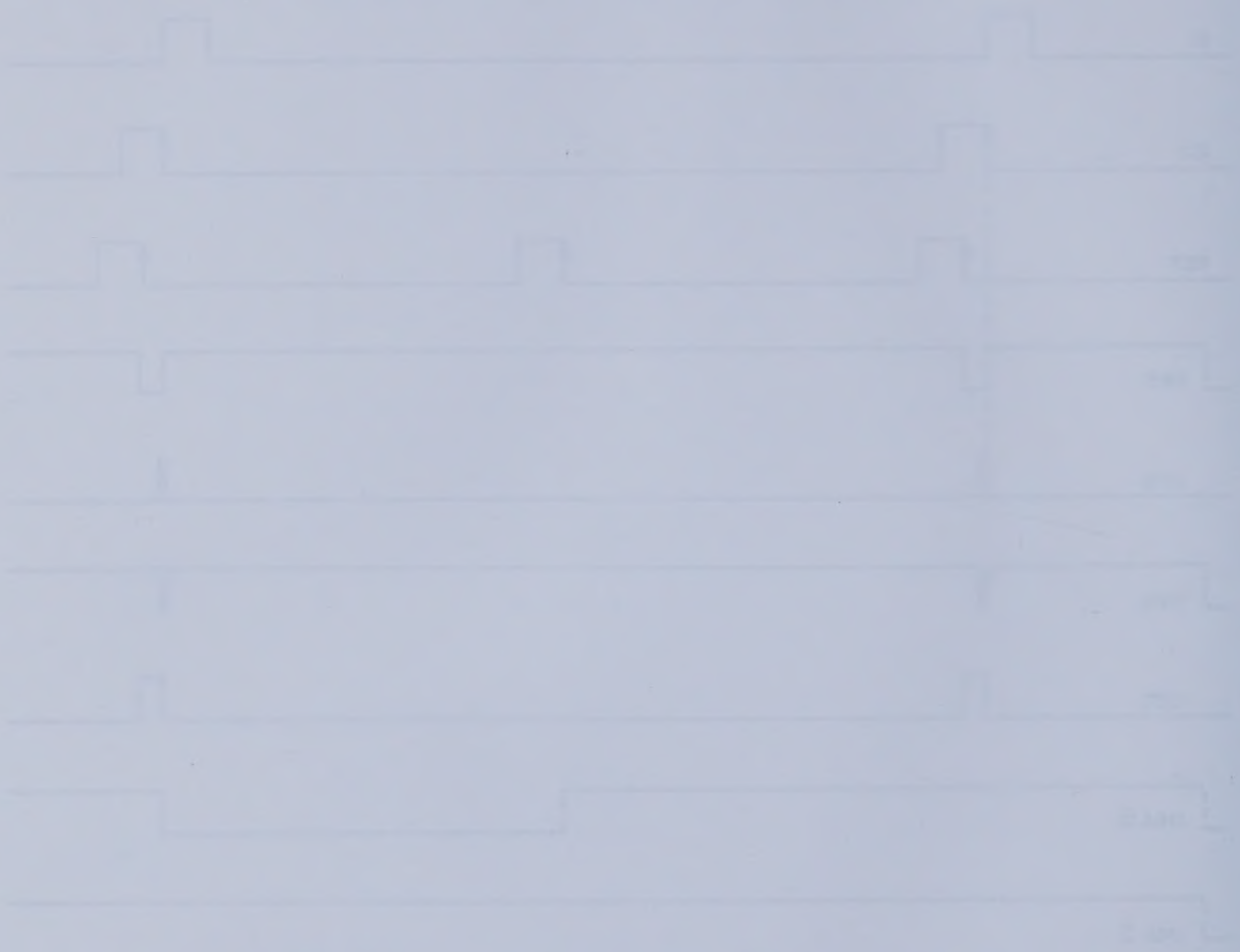


Figure 5-12. Variable Reference Frequency Loop Frequency-Phase Frequency-Phase Detector and Ramp Generator Control Waveforms.



The charge on capacitor C57 controls the conduction of Q10. The conduction of Q10 determines the output of operational amplifier U24A. The output of U24A is the dc tuning voltage applied to voltage variable capacitors CR3 and CR4 to control the operating frequency of the VCO.

The logic 0 to 1 transition of Ø2 is also used to clock U7B to the reset condition, this, through U8B and U8C will provide forward bias for Q4. With Q4 conducting, Q5 conducts, discharging C27. Q4 and Q5 will conduct until U7A flip-flop is clocked.

The fixed reference divider receives an input of 39.6 MHz at A5A2P3 from the frequency standard. The signal is squared by Q1 and applied to U1A. U1A and U1B provide a divide-by-four function and supply the clocking signal to U2 and U3. U2 and U3, divide-by-9 and divide-by-11, provide a divide-by-99 function. The QC output of U3, pin 12, is the 100-kHz signal clocking U4A while the QD output, pin 11, is the 100-kHz reference input to the translator loop frequency phase detector. U4A, divide-by-10, U4B divide-by-10 and U5B, divide-by-2, produce the 500-Hz signal that is the clock for U7A and U6A in the frequency phase detector.

With the variable reference frequency loop operating properly, in a locked condition, U6A will always be clocked when the D input is logic 0 and U6B will always be clocked when the D input is logic 0. For this to occur the two input signals to the frequency phase detector, Ø2 and the output of the fixed reference divider must alternate.

As long as the inputs continue to arrive at the detector alternately U6A and U6B will remain in the reset condition, giving a logic 1 output from U6A $\overline{Q}$ to J1, pin 6, which indicates the synthesizer is operating in a locked condition. The previously discussed lock monitor (LM) output from loops 1 and 2 is an input to A5A2P1, pin 9, applied to the set input of U6B. If a loss-of-lock occurs in loop 1 or loop 2 the LM input will be logic 0, setting U6B which will set U6A giving a logic 0, fault indication, on the LOL output.

5.4 OSCILLATOR ASSEMBLY A7 ANALYSIS

Refer to the oscillator assembly schematic. The oscillator assembly A7 contains three crystal-controlled oscillators that provide an injection frequency to the receiver-exciter, a frequency standard input to the synthesizer and two bfo frequencies to the receiver-exciter.

Oscillator Q1 is enabled whenever the +5-V dc is applied to A7. The 39.6-MHz crystal Y3 and variable capacitor C15 determine the operating frequency of the oscillator. C15 is adjusted for an oscillator frequency of 39.6 MHz ±3 Hz. From the collector of Q1 the signal is coupled through C21 to J2, this signal is input to the fixed divider in the synthesizer where it is divided down to produce the frequency standard for the synthesizers phase-locked loops. Another output from oscillator Q1 is through C22 to the base of amplifier Q2. From the collector of Q2 the signal is filtered and output from A7 at P1. This output is routed to receiver-exciter board A3, where it is used as an injection to the first transmit mixer and the second receive mixer.

The 454.2-kHz oscillator is enabled by a logic 1 applied at pin 8 from the receiver-exciter card A3. With a logic 0 at pin 8 the output of U19 pin 11 is held at a steady logic 1 to disable the oscillator. When enabled by a logic 1 at U1D, pin 12, the oscillator will oscillate at the frequency of crystal Y2, 454.2 kHz. The output is taken from U1D, pin 11, and input to inverter U2F. U2F provides isolation between the oscillator and the output. The signal is inverted at U2F, filtered, and output from the A7 assembly at P3. The 454.2-kHz is used in the product detector and to generate the 800-Hz SPOT-signal in A3.

The 455-kHz oscillator is enabled by a logic 1 at pin 6 from the A3 board. The logic 1 applied to U1C, pin 9, enables the NAND gate and the oscillator oscillates at the 455-kHz frequency of crystal Y1. Variable capacitor C7 is used to adjust the oscillator frequency to within ±3 Hz of 455 kHz. The output of the oscillator taken from pin 10 of U1C is inverted by U1B and applied to NAND gate U1A. With a logic 0 at CW KEYING input, pin 4, the output of U1A is held at a constant logic 1, blocking the output of the oscillator. With a logic 1 applied to pin 4 from the A3 board, U1A is enabled and the signal is applied to U2C. At the output of U2C the 455-kHz is filtered and output from the A7 assembly at P2. The output at P2 is routed to the A3 board where it is used as the carrier injection during CW transmit operation, the injection to the product detector during SSB receive operation and to generate the 800-Hz SPOT frequency.

5.5 SELF-TEST

1. The loop 2 VCO output frequency is varied by changing the _____ _____ of the variable divider.

2. With the KWM-380 set for 00.5000 MHz, receive operation, the loop 1 VCO output frequency is _____ MHz.

3. With 00.50000 MHz, receive operation the division ratio of the loop 2 divider is _____.

4. The minimum division ratio of the variable reference frequency divider is _____ _____ and the maximum is _____.

5. With an operating frequency of 29.99999 MHz the binary frequency information at U22 will be:

   pin 4 = logic _____
   pin 5 = logic _____
   pin 6 = logic _____
   pin 7 = logic _____
   pin 14 = logic _____
   pin 13 = logic _____
   pin 12 = logic _____
   pin 11 = logic _____

6. With an operating frequency of 28.000000 MHz, the binary frequency information at U18 will be:

   U18 pin 7 = logic _____
   pin 14 = logic _____
   pin 13 = logic _____
   pin 12 = logic _____
   pin 11 = logic _____

5.6 SELF-TEST ANSWERS

1. Division Ratio

2. 39.645 MHz

3. 362

4. Minimum = 294500

   Maximum = 394499

5. pin 4 = logic 0

   pin 5 = logic 1

   pin 6 = logic 0

   pin 7 = logic 1

   pin 14 = logic 0

   pin 13 = logic 0

   pin 12 = logic 0

   pin 11 = logic 0

6. pin 7 = logic 0

   pin 14 = logic 0

   pin 13 = logic 1

   pin 12 = logic 1

   pin 11 = logic 1

VOX OUT	A3J12/P12-12 to S7B, front panel VOX switch. Logic 1 or 0. Logic 0 output from A3 with key output from VOX circuit.
NB ENBL	A3J12/P12-13 to S7C, front panel NB switch. +9 V dc from S7C to A3 with NB (noise blanker) switch depressed.
PROC ENBL	A3J12/P12-14 to S7D, front panel PROC switch. +9 V dc from S7D to A3 with PROC (processor) switch depressed.
AGC OFF	A3J12/P12-15 to S7E, front panel AGC switch. +5 V dc from S7E to A3 with AGC (automatic gain control) switch not depressed. With switch depressed (AGC on) 0 V applied to A3.
AGC SLOW	A3J12/P12-16 to S7F, front panel SLOW switch. +5 V dc from S7F to A3 with SLOW switch not depressed, 0 V dc, slow AGC action, with switch depressed.
PTT	A3J12/P12-17 to S3, front panel VFO select switch. Logic 1 or 0. Logic 1 with PTT (push-to-talk) signal present.
$\overline{\text{SPOT}}$	A3J12/P12-80 to S2, front panel SPOT switch. Logic 1 or 0. Logic 0 with spot button depressed (spot circuits activated).
+5 V dc	A3J12/P12-19 to S7E, front panel AGC switch. Provides +5 V dc to S7E.
VOX A	A3J15/16-S to S7B output from front panel VOX switch to U910A on A3.
VOX B	A3J15/P15-6 to S7B input to front panel VOX switch from U913A on A3. Input is logic 1 with CW selected and key down.
	Refer to schematic sheet 3.
SAFETY GND -12 V dc	A9J1-9 to ground.
115/230 V ac (H) or +V dc	A9J1-11 to TB1-X. Primary power path through on-off switch and fuse F1.
115/230 V ac (L) and FAN AC	A9J1-7 to P2-9. 115/230 V ac return through on-off switch.
FAN AC	A9J1-12 to P2-6. Ac power from chassis to operate external cooling fan.
+12 V dc to JUMPER	A9J1-10 to TB1-X. +12 V dc to TB1 through fuse F2.
+12 V dc from JUMPER	A9J1-8 to VR2. +12 V dc from jumper on A9 chassis.
PWR GND	A3J14/P14-1 to A9A2-E4. Ground connection between chassis and A3 module.
+24 V dc	A3J14/P14-3 to A9A2-E3. +24 V dc from power supply to A3.

6.1 OBJECTIVES

6.2 BLOCK DIAGRAM ANALYSIS

Figure 6-1

6.3 POWER SUPPLY CIRCUIT DESCRIPTION

6.4 SELF-TEST

6.5 SELF-TEST ANSWERS

6.1 OBJECTIVES

This section of the self-study manual provides an overall view and a detailed circuit description of the KWM-380 Power Supply. At the completion of this section, the student should have accomplished the following:

a. Know the changes required to operate the transceiver from various ac power sources or a dc source.
b. Understand the operation of the +14-V regulator.
c. Be familiar with the operation of the +9-V regulator.
d. Know the operation of the +5-V regulators.
e. Understand the operation of the +24-V switching regulator.

6.2 BLOCK DIAGRAM ANALYSIS

Refer to figure 6.1. The power supply in the KWM-380 contains five voltage regulator circuits, +14, +9, +24, and two +5 volts. The +14-V regulator, in addition to providing the +14-volt output also supplies the input to the other four regulators. Transformer T1, current sense resistors R5 and R6, zener diode VR2, and regulator U1 are mounted on the KWM-380 chassis, A9. The +14-V series-pass transistors, Q1-Q3, and the thermal switch are mounted on heat sink A1. The control circuits for the +14-V regulator, U1B, U1A, and Q1 are mounted on power supply control card A9A1. These circuits monitor the output current and voltage and provide feedback to the series-pass transistors to maintain proper output. The +9- and +5-volt regulators operate with +14 volts in while producing regulated +9 and +5 V outputs. The output from the +14 regulator is also input to the +24-volt switching regulator located on A9A2. The switching regulator is a shunt (step-up) type which increases the voltage before it is regulated at +24 V by a zener diode.

6.3 POWER SUPPLY CIRCUIT DESCRIPTION

Refer to block diagram figure 6-1 in the self-study manual and the power supply schematic in the KWM-380 Service Manual.

The primary power input to the power supply is at connector J1 on the rear of the KWM-380. For ac operation, 50 to 60 Hz, 105 to 250 volts the inputs are J1, pin 7, neutral, pin 11, high and pin 9 safety ground. For dc operation, 12 to 15 V, the inputs are, pin 9, common, pin 11, +12 to 15 volts with 8 and 10 jumpered together. Pin 12 is a switched 115 V ac output for operating a blower. For either ac or dc operation switch S1 on the front panel controls the application of primary power to the regulator circuits. Fuse F1 provides protection during ac operation and is rated at 4A with 230 volts input and 8 amps with 115 volts input. F2 provides protection during dc operation and is rated at 30 amps.

When operating from an ac source, closing switch S1 applies power to terminal board TB1 through fuse F1. TB1 is the point where strapping is done to allow the KWM-380 to operate with various ac voltages. See note 6 on the power supply schematic or table 1-4 in this manual for strapping directions. The ac voltage at TB1, primary of T1, is coupled to the full-wave

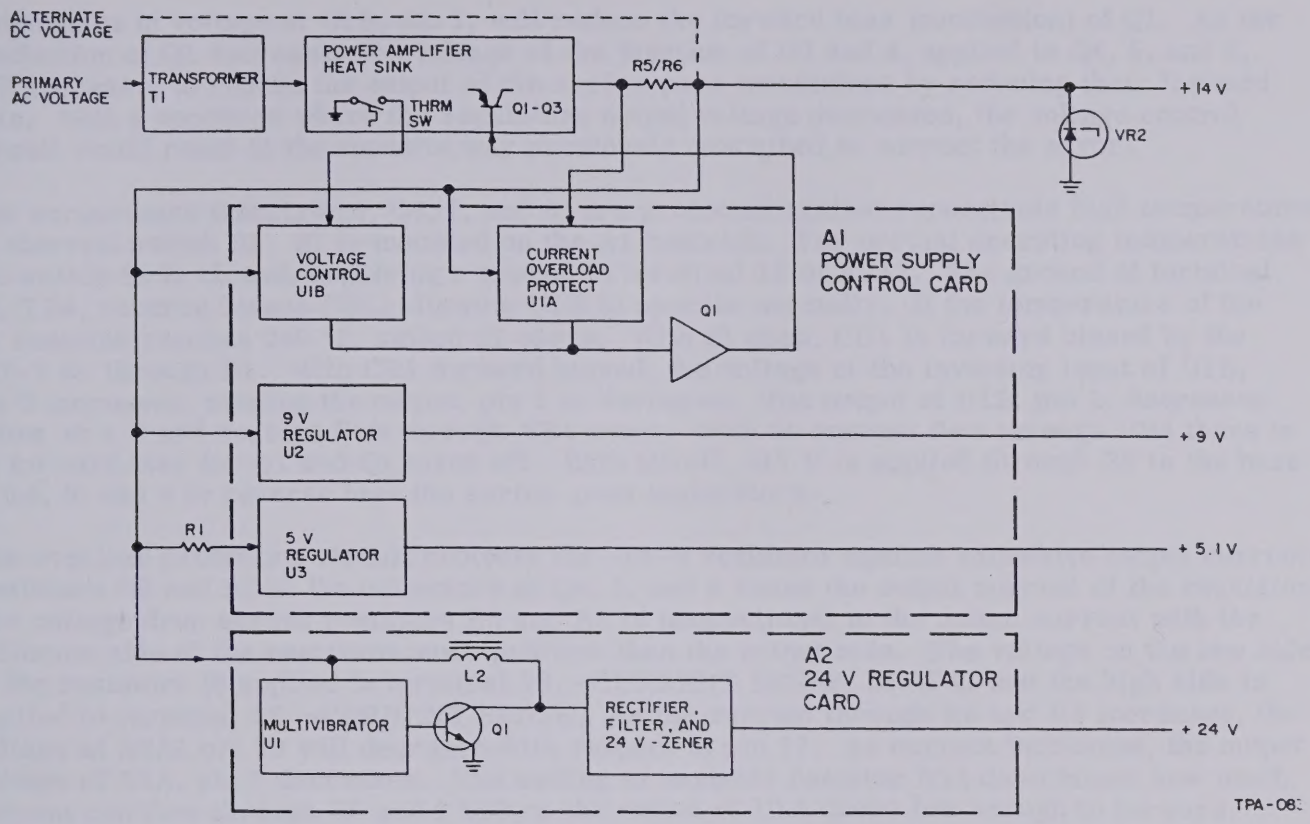


Figure 6-1. Power Supply Block Diagram.

rectifier at the secondary of center tapped transformer T1. The output of the full-wave rectifier, at the cathodes of CR1 and CR2 is +17 V dc. This unregulated +17 V is applied t the emitters of Q4, Q5, and Q6, and to power supply control card A2A1. Resistors R2, R3, and R4 are dropping resistors used to reduce the power dissipation of Q4, Q5, and Q6. A4 and 6 are series-pass regulators connected in parallel to increase their current capability The conduction of Q4, 5, and 6 is controlled by the overload protection and voltage control circuits on power supply control card A2A1, to regulate the output, collector, voltage of Q 5, and 6 at +14 V dc.

Voltage regulation is accomplished by sampling the regulator output and applying it to ter nal 16 on A2A1. A portion of this voltage, determined by the setting of R23 in voltage divi R23, R22, and R19, is applied to the inverting input, pin 2, of differential amplifier U1B. set voltage at the noninverting input, pin 3, is regulated at +6.2 V by zener diode VR1. Th output of U1B, pin 1, a positive voltage greater than +2.4 V, controls the conduction of Q1. By controlling the conduction of Q1, the voltage at the junction of R3 and R4 leaves the A2 card at terminal 21 and is applied to the bases of series regulator Q4, 5, and 6 on A1 thro terminal E4. This voltage controls the conduction of Q4, 5, and 6 to maintain a regulated output voltage of +14 V dc. Variable resistor R23 is the +14-V adjust.

The following is an example of the +14-V regulator operation. During transmit operation 5, and 6 are forward biased sufficiently to provide 25-30A at +14 V. When the transceiver switches from transmit to receive, the current requirement decreases and the output volt will tend to increase. This increase is sampled by R19, 22, and 23, increasing the voltage U1B, pin 2. Because U1B, pin 2, is the inverting input and pin 3 the noninverting input is constant, the output voltage of U1B pin 1 will decrease.

A decrease in voltage at U1B, pin 1, will reduce the forward bias (conduction) of Q1. As the conduction of Q1 decreases the voltage at the junction of R3 and 4, applied to Q4, 5, and 6, will increase, to reduce the output of the series-pass transistors by reducing their forward bias. With a condition where the regulators output voltage decreases, the voltage control circuit would react in the opposite way previously described to correct the error.

The series-pass transistors, Q4, 5, and 6, are protected against excessively high temperatures by thermal switch S1. S1 is mounted on the A1 heatsink. For normal operating temperatures the switch S1 is closed, supplying a ground to terminal 18 of A9A1. The ground at terminal 18, TP4, reverse biases CR1, allowing U1B to operate normally. If the temperature of the A1 heatsink reaches 240 °F, switch S1 opens. With S1 open, CR1 is forward biased by the +17-V dc through R1. With CR1 forward biased, the voltage at the inverting input of U1B, pin 2 increases, causing the output, pin 1 to decrease. The output of U1B, pin 1, decreases below +2.4 V and current flow through VR4 stops. With no current flow through VR4 there is no forward bias for Q1 and Q1 turns off. With Q1 off, +17 V is applied through R3 to the base of Q4, 5, and 6 to reverse bias the series-pass transistors.

The overload protection circuit protects the +14-V regulator against excessive output current. Resistors R5 and R6 at the collectors of Q4, 5, and 6 sense the output current of the regulator. The voltage drop across resistors R5 and R6 is proportional to the output current with the collector side of the resistors more positive than the output side. The voltage on the low side of the resistors is applied to terminal 19, -CURRENT SENSE, of A2A1 and the high side is applied to terminal 17, +CURRENT SENSE. As the current through R5 and R6 increases, the voltage at A2A1 pin 19 will decrease with respect to pin 17. As current increases, the output voltage of U1A, pin 7 decreases. The setting of variable resistor R16 determines how much current can flow through R5 and 6 before the output of U1A drops low enough to forward bias CR2. R16 is factory adjusted to initiate current limiting at 30 amps. With CR2 forward biased, current flows through CR2 and R7 reducing the voltage at the junction of R7 and VR4. As the voltage at the cathode of VR4 drops, the conduction of Q1 decreases, reducing the forward bias of Q4, 5 and 6 to limit the output current.

The output of the regulator is supplied directly to the pa (high I + 14 V dc) and also to terminal 11 of A2A1 (TP6). From pin 11 the voltage applied to terminal 12 through a 2A fuse, F2 and to terminal 10 through a 2A fuse F1 and R31. From pins 10 and 12 the +14-V is distributed to various sections of the transceiver via the chassis.

The +14-V input at terminal 11 of A2A1 is also applied to A2A1L1, the input to the +9- and +5-V regulators. The +9-V regulator consists of U2, R11, R27, R12, C7, and C8. U2, an LM 317, is an adjustable 3-terminal positive voltage regulator, capable of supplying 1.5 A with an output voltage range of 1.2 to 37 V. The integrated circuit regulator has internal current limiting, thermal protection and output voltage regulation of 0.01 percent per volt. The output voltage of U2, pin C, is sampled by resistive voltage divider R11, R27, and variable resistor R12. R12, +9-V adjust, controls the output voltage by controlling the input voltage at the adjustment input, pin 1, of U2. The regulated +9 V dc from U2, TP2, leaves the A2A1 card at terminals 7 and 8 for distribution throughout the transceiver.

The +14-V input to U2 is also applied to terminal 13. From terminal 13, the voltage is routed through chassis mounted resistor R1 and back to the A2A1 card at terminal 1. R1 is a voltage dropping resistor used to reduce the power dissipated by the 5-V regulator, U3. From terminal 1 of A2A1 the input voltage is applied to pin 2 of U3. The operation of U3, +5-V regulator, is the same as the previously discussed 9-V regulator. Variable resistor R14 adjusts the regulator adjustment input of U3, pin 1, to produce a regulated +5-V at TP1 that is applied to terminals 3 and 2 for distribution throughout the transceiver. The chassis mounted, 6.2-V zener diode, VR1, connected to terminal 2 provides protection for circuits external to the power supply against transients and high voltage caused by the failure of U3.

The output of the +14-V regulator is applied to 24 V dc switching card A2A2 at terminal 1. A2A2 is a shunt (step-up) switching voltage regulator. U1, a μA555 timer, is used to drive switching transistor Q1. With pins 2 and 6 tied together U1 will trigger itself and free run as a multivibrator. While capacitor C2 is charging, through R1, R2, and R3 the output of U1 pin 3, is high, providing forward bias for Q1. While C2 is discharging through R2 and R3, the output of U1, pin 3, is low, reverse biasing Q1. Because of the different charge and discharge paths for C2 the resistance ratio between R1, and R2, and R3 determines the duty cyc of the output at pin 3. The reset function of U1, pin 4, is disabled by the +14-V applied to it. The +6.2-V at the junction of VR1 and R4, U1 pin 5, provides compensation to keep the outpu of the regulator constant with variations of the applied input voltage.

During the charging cycle of inductor L2, the period of time when Q1 is forward biased, L2 is fed directly by the applied +14-V. While L2 is charging, diode CR1 is reverse biased and does not allow the current in the inductor to supply any contribution of current to the load. During this time, capacitor C4 is the primary source of current for the load. When Q1 turns off, diode CR1 is forward biased and the discharge of L1 provides load current and charging current for capacitor C4. The output of the regulator is filtered by L3, C5 and C6 and is limited to +24 V dc by zener diode VR3. The regulated +24-V dc is distributed throughout the transceiver.

A9U1, a chassis-mounted +5-volt regulator receives its input from the +14-V line and suppli a regulated +5-volts to control card A8. The use of a seperate regulator for A8 ensures tha the microprocessor circuits on A8 are isolated from other circuits operating on +5 volts.

With dc operation the +14-volt regulator is bypassed. At this time VR2, on chassis A9, provides transient and reverse polarity protection. The operation of the +9-, +5- and +24-volt regulators is the same with dc operation as previously described for ac.

6.4 SELF-TEST

1. With A9A1R16 properly adjusted, current limiting will not occur in the +14-V regulator until the voltage drop across R5 and R6 reaches _____ V dc.

2. With thermal switch S1 closed (normal operation) the voltage at TP4 is _____ V.

3. If capacitor C7, in the +9-V regulator, shorts, the output voltage will _____.

4. If Q1, in the +24-V regulator, opens, the output voltage of the regulator will _____.

5. If VR3 opens, the output of the +24-V regulator will _____.

6. With the KWM-380 operating from a dc source, the _____ V regulator is not used.

7.1 OBJECTIVES

7.2 GENERAL DESCRIPTION

Figure 7-1

Figure 7-2

7.3 CONTROL CARD DETAILED THEORY

Figure 7-3

Figure 7-4

Table 7-1

Figure 7-5

7.4 A10 DISPLAY BOARD THEORY

Figure 7-6

7.5 SELF-TEST

7.6 SELF-TEST ANSWERS

7.1 OBJECTIVES

This section of the self-study manual provides information on the A8 control card and the front panel display board. At the completion of this section the student should have accomplished the following:

a. Know the control inputs to the control card.
b. Have a basic understanding of the operation of the microprocessor circuitry.
c. Know the correct parallel outputs from the control card.
d. Have an understanding of the serial frequency information output of the control card.
e. Know how the frequency information is displayed in the front panel display.

7.2 GENERAL DESCRIPTION

Refer to figures 7-1 and 7-2.

The control board takes frequency data from the front panel or optional external keypad and develops output signals. These output signals supply: serial format frequency data to the synthesizer, parallel format data to the front panel frequency display and a remote device, selection control for the low-pass filters, and an inhibit signal to the transmitters. (Refer to figure 7-1.) A microprocessor with associated ROM, decoders, and latches processes the input data to develop the output signals.

Figure 7-2 is a flow chart showing the basic operation of the microprocessor. When power is applied, the microprocessor resets and initializes to output 15.000 00 MHz frequency data. Internal instructions then command the input data lines to be polled until a frequency change is sensed. When tuning knob or remote keypad frequency data is received, this data is added to or subtracted from the last frequency data in the microprocessor. The new result causes the control board outputs to change to the new frequency data. The microprocessor then returns to the polling routine until it senses another change in input data.

7.3 CONTROL CARD DETAILED THEORY

Refer to block diagram figure 7-1, 7-2, 7-3 and 7-4 in the self-study manual and the control card schematics sheets 1 and 2 in the service manual.

The central processor unit (CPU) in the KWM-380 is the 6802 type. It is driven by an external clock; has a parallel 8-bit bidirectional data bus; a parallel 16-bit undirectional address bus (with bits A11 and A12 unused); and clock (Ø2), read/write (R/W), and valid memory address (VMA) control signals. An internal 128 X 8 bit RAM permits storing operating frequencies for the A and B vfo's.

When power is first applied to the control board, the charging time constant of C2 and R1, to the +5-V dc line, keeps a logic 0 on the CPU $\overline{\text{Reset}}$ input, pin 40, through inverts U9E and U9D for approximately 1 second. The logic 0 at the $\overline{\text{Reset}}$ input of the CPU resets the CPU and

causes an output to be generated that will develop a 15.000 00-MHz output data. This initializes the circuits to 15-MHz each time power is applied regardless of the previous operating frequency.

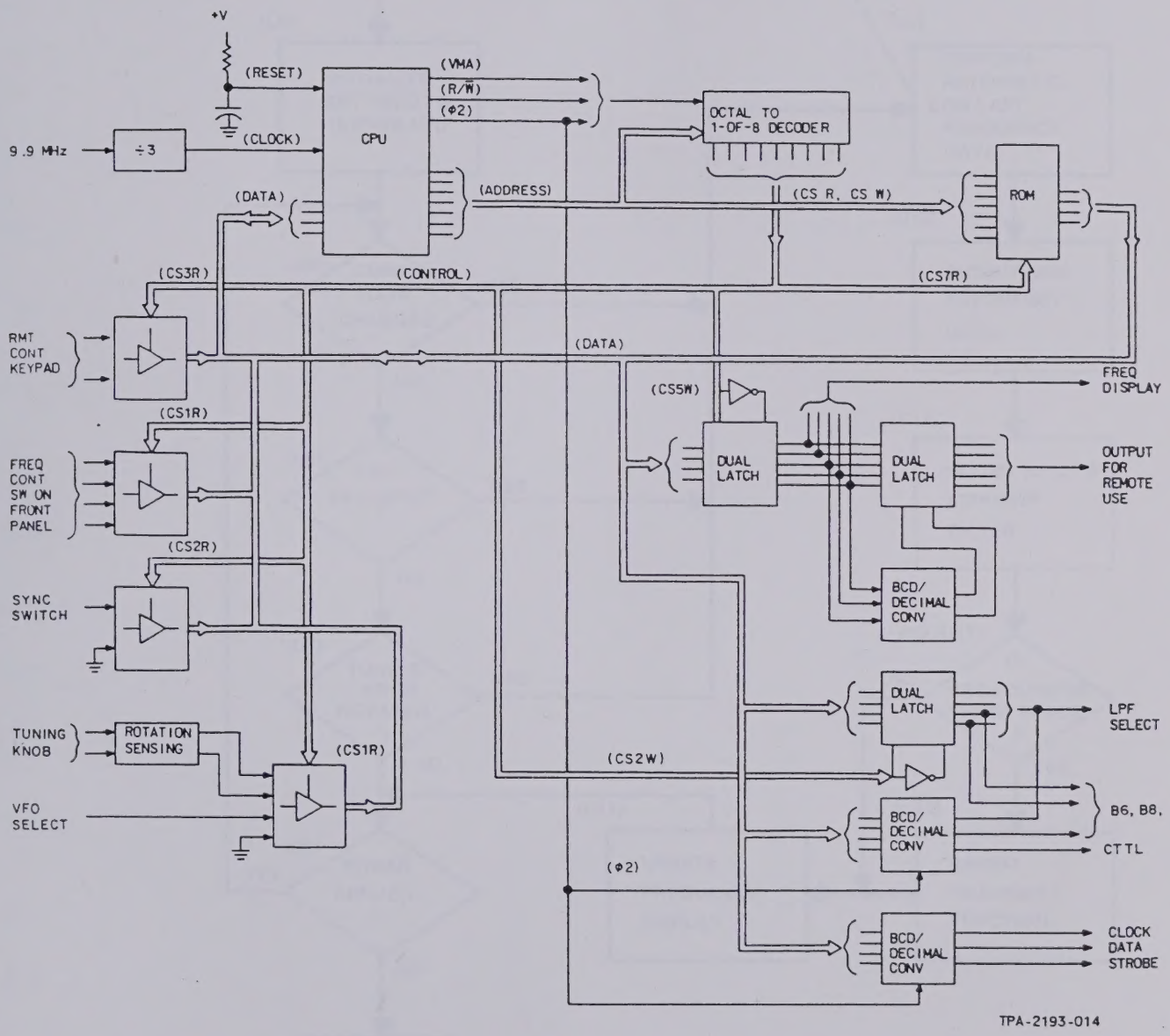


Figure 7-1. Control Card A8 Block Diagram.

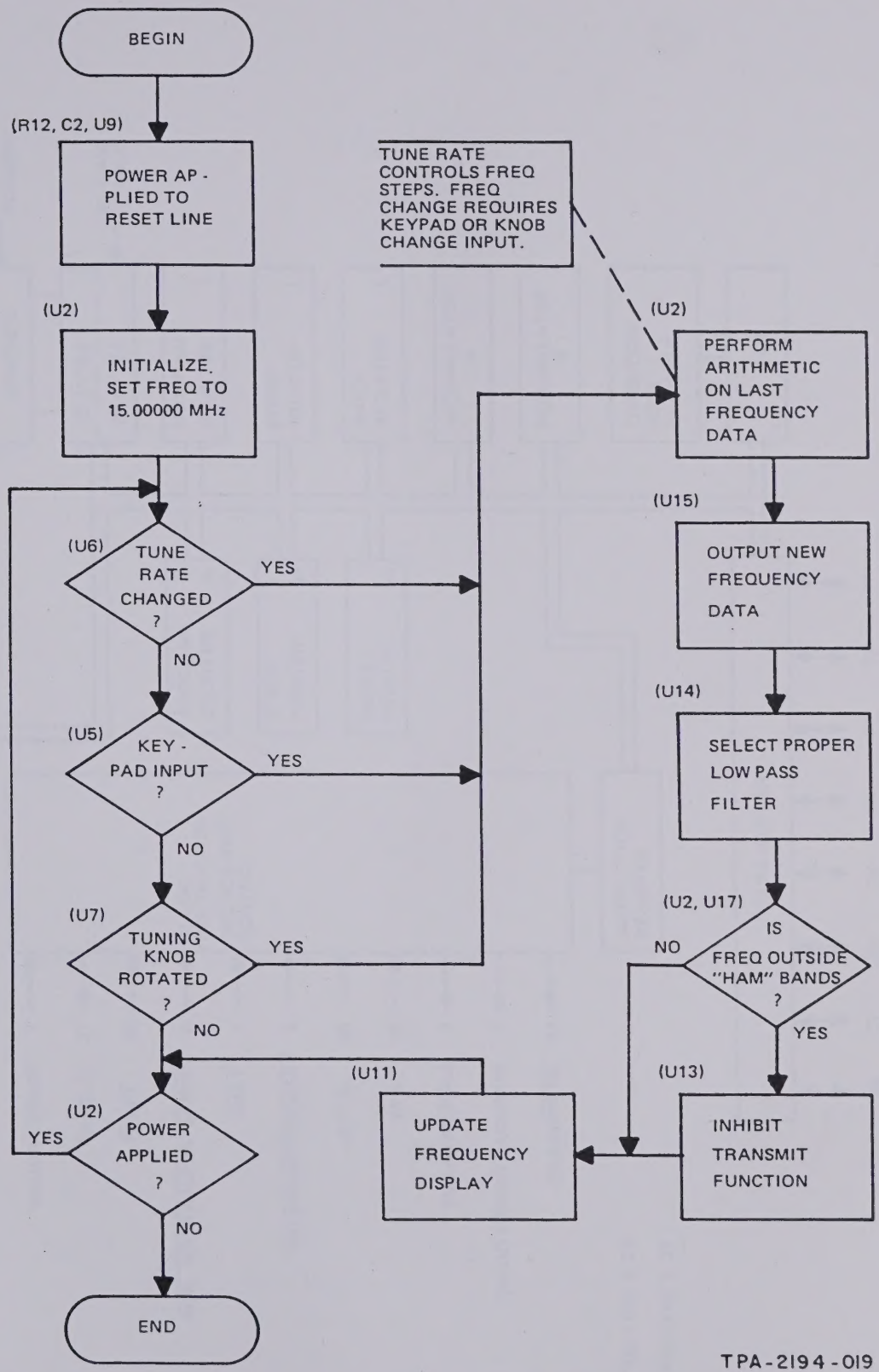
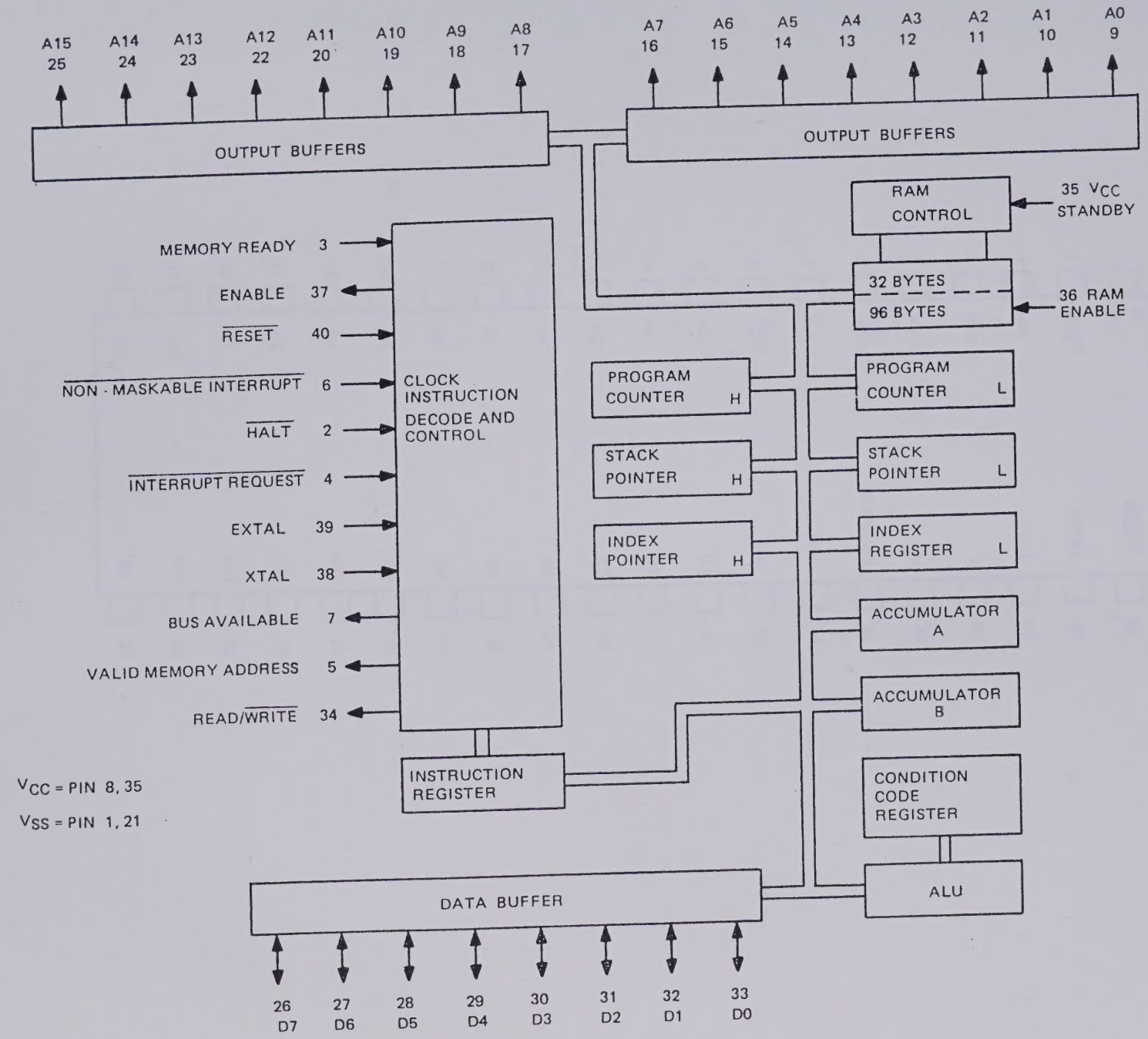


Figure 7-2. Microprocessor Operation Flow Chart.


A15 25
A14 24
A13 23
A12 22
A11 20
A10 19
A9 18
A8 17
A7 16
A6 15
A5 14
A4 13
A3 12
A2 11
A1 10
A0 9
OUTPUT BUFFERS
OUTPUT BUFFERS
RAM CONTROL
35 VCC STANDBY
32 BYTES
96 BYTES
36 RAM ENABLE
MEMORY READY 3
ENABLE 37
RESET 40
NON-MASKABLE INTERRUPT 6
HALT 2
INTERRUPT REQUEST 4
EXTAL 39
XTAL 38
BUS AVAILABLE 7
VALID MEMORY ADDRESS 5
READ/WRITE 34
CLOCK INSTRUCTION DECODE AND CONTROL
PROGRAM COUNTER H
PROGRAM COUNTER L
STACK POINTER H
STACK POINTER L
INDEX POINTER H
INDEX REGISTER L
ACCUMULATOR A
ACCUMULATOR B
INSTRUCTION REGISTER
CONDITION CODE REGISTER
ALU
DATA BUFFER
VCC = PIN 8, 35
VSS = PIN 1, 21
26 D7
27 D6
28 D5
29 D4
30 D3
31 D2
32 D1
33 D0

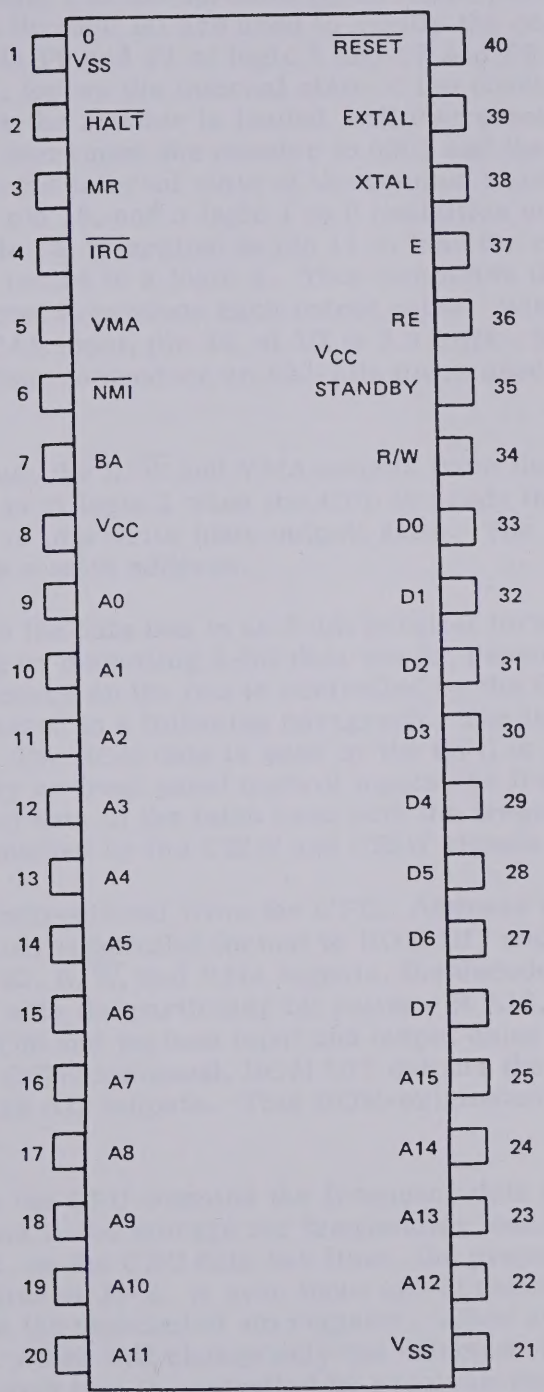


Figure 7-4. Microprocessor Pin Identification.

The CPU clock is derived from the 9.9-MHz output from the synthesizer. The 9.9-MHz enters the control board at J9 and is applied to the clock input, pin 14 of counter U1. Clock enable (CE) is grounded to enable the counter. The clocking occurs on a logic 0 to 1 transition at the clock input. The logic 1 at the $\overline{up}$/down ($\overline{U}$/D) input, pin 5, causes the counter to count down. The input at P0 through P3 are used to modify the count sequence of U1 to make it divide by 3. With inputs P0 and P1 at logic 1 and P2 and P3 at logic 0, a logic 0 applied to load input (PL), pin 11, forces the internal state of the counter to binary 3 (0011). The first clock pulse to U1, after the counter is loaded, will decrement the counter by one to 0010. The second clock will decrement the counter to 0001 and the third clock will decrement the counter to 0000. When the internal state of the counter reaches 0000, a logic 0 to 1 transition occurs at output (TC), pin 12, and a logic 1 to 0 transition occurs at ripple clock output (RC), pin 13. The logic 0, pin 13, is applied to pin 11 to load the counter to 0011 again, which causes the output at pin 12 to return to a logic 0. This completes the count sequence of U1, three input pulses are required to produce each output pulse. With an input of 9.9 MHz to U1, the output, applied to EXTAL input, pin 39, of U2 is 3.3 MHz. Internal circuits in the CPU divide the 3.3-MHz input by four to produce an 825-kHz clock used internally in the CPU and output from the CPU as Ø2.

Along with the Ø2 output, the R/$\overline{W}$ and VMA outputs from the CPU are also applied to decoders U3 and U4. The R/$\overline{W}$ is at logic 1 when the CPU is ready to read data. This signal goes to a logic 0 when the CPU is in a write (data output) state. The VMA output is logic 1 when the CPU address output is a valid address.

Data is transferred on the data bus in an 8-bit parallel format. The CPU data bus lines are bidirectional inputting or outputting 8-bit data words, depending on the CPU internal operating mode. Input data presence on the bus is controlled by the CSIR, CS2R, CS3R, and CS7R control signals, discussed in a following paragraph. The input is from the ROM, keypad, or front panel controls. The ROM data is used by the CPU in processing data to be output to external circuits. Key or front panel control inputs are frequency data to the CPU. The bus applies the CPU output data to the latch used with the frequency display and the latches and converters must be enabled by the CS2W and CS5W signals before outputting the bus data.

The address bus is undirectional from the CPU. Address bits A0 through A10 and A13 through A15 are applied in parallel format to ROM U17 and decoders U3 and U4 respectively. When enabled by the Ø2, R/$\overline{W}$, and VMA signals, the decoders output the chip select (CSXX) command associated with the particular bit pattern of A13, A14, and A15. These commands select (enable) the ROM and various input and output chips (integrated circuit components). When enabled by the CS7R command, ROM U17 outputs the data stored in the location addresse by the CPU A0 through A10 outputs. This ROM-originated data word is input, through the data bus, to the CPU.

The internal RAM in the CPU contains the frequency data processed from the front panel or keypad controls. This is the storage for frequencies loaded into the A and B vfo registers. The RAM will output, on the CPU data bus lines, the proper stored frequency as requested by the vfo select input line at J6-3. A sync input (J6-5) causes the CPU to store the frequency of the selected vfo in the unselected vfo register. After syncing the frequencies, a new frequency may be input which will change only the selected vfo frequency. In split-frequency operation, the vfo select line is controlled by receiver-exciter logic circuits to automatically select the proper vfo for receive or transmit.

When power is turned off, all data in the RAM is dumped. The ROM, U17, is a 2048 x 8-bit memory containing a look-up table and instructions for the CPU. The look-up table supplies constants necessary for computation within the CPU. The instructions tell the CPU what to do with the previous data that has been input to the CPU.

When the CS7R output from U3 goes to logic 0, the ROM is enabled. The A0 through A10 word from the address bus addresses a particular location in the ROM. Data stored in that memory address is output to the data bus as the D0-D7 word. This data is received by the CPU for use in internal processing of the data. At the time the ROM-originated data word is on the data bus, no other chip is selected so no invalid outputs are developed and applied to circuits external to the control board. Only the processed CPU output data is applied from the data bus through the latches and decoders to the circuits.

Three-line to eight-line decoder U3 and U4 develops the chip select read and write commands. The decoders will both be simultaneously addressed by bits A13, A14, and A15. Unless VMA is logic 1 and Ø2 and R/$\overline{W}$ at the decoder inputs are logic 0, all the decoder outputs will be logic 1 regardless of the A13 through A15 inputs.

Referring to the schematic diagram and following the logic levels, it is seen that the U3 outputs are controlled by the address line inputs when R/$\overline{W}$ is logic 1 and Ø2 is logic 0. Inverter U10B causes the logic 1 R/$\overline{W}$ to be applied to U3 as logic 0. This satisfies the input control line conditions that enable developing an output from the address inputs. The U3 outputs are chip select read, CSxR, commands. (Note that the read commands are developed when the R/$\overline{W}$ control line is logic 1.) Decoder U4 similarly develops chip select write, CSxR, commands when R/$\overline{W}$ is logic 0. Table 7-1 shows the chip select output for each input address.

Table 7-1. Chip Select Outputs for Input Addresses.

ADDRESS			U3 OUTPUTS					U4 OUTPUTS			
A15	A14	A13	CS1R	CS2R	CS3R	CS6R	CS7R	CS2W	CS3W	CS5W	CS6W
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	1	0	1	1	1	0	1	1	1
0	1	1	1	1	0	1	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	0	1
1	1	0	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1

Front panel control or keypad data is transferred to the data bus through tri-state buffers U5, U6, and U7. Before the buffer will transfer data, the buffer enable signal must be logic 0. When the enable signal is logic 0, the input logic level is transferred directly through the buffer to the data bus. A logic 1 enable signal causes the buffer output to the bus to be at a high level of impedance regardless of the input logic level. The enable signals are the CS1R, CS2R, and CS3R outputs from decoder U3.

When CS1R is logic 0, parts of buffers U6 and U7 are enabled. Any input from the frequency tuning increment switches (SLOW (10 Hz), MED (100 Hz), FAST (1 kHz), or BAND (1 MHz)), tuning knob, or VFO SELECT switch is applied to the data bus. These inputs are data bits D0 through D3 and D5 through D7 respectively. Bit D4 is hard wired to logic 0.

The frequency tuning knob inputs are developed from an optical encoder located on the chassi As the tuning knob is rotated, light beams are chopped into pulses that are applied to the A8 board at J6 pins 1 and 2. Input pulse A, J6-1, will precede pulse B, J6-2, when the tuning kn is rotated counterclockwise, and vice versa. Refer to figure 7-5. The B input is inverted by U9A and applied to the clock (C) input of flip-flop U8B, pin 11, and inverted again by U9B before being applied to pin 4 of U7. The A input is inverted by U9F and applied to the D inpu of U8B, pin 9. When a clock pulse is applied to U8B, a logic 0 to 1 transition, the logic level at the D input will appear at the Q output. With the A pulse leading the B pulse at J6, the clo to U8B will occur when the D input is at logic 0, this will reset the flip-flop, producing a logi 0 output at Q, pin 13. With the B pulse leading the A pulse at J6, input D will be high when th clock occurs, causing U8B to set, producing a logic 1 output at Q. The Q output of U8B is inverted by U9C and applied to pin 6 of U7 (D6). With U7, pin 6 (D6) at logic 0, the pulse stream applied to U7, pin 4, (D5) will cause the CPU to increase in frequency from the frequency already in the RAM. The size of the frequency increment is determined by the logic levels input to the A8 card at J6, pins 7, 8, 9, and 10. These inputs, 10's Hz, 100's Hz, 1's kHz and 1's MHz, originate at the front panel frequency control switches.

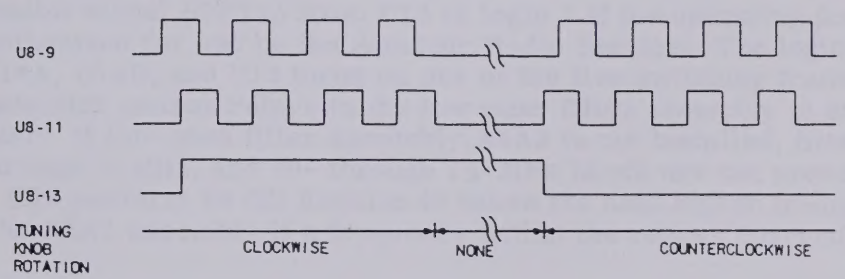


Figure 7-5. Tuning Knob Rotation Sensor Waveforms.

When CS2R is logic 0, SYNC buffer U7-12 is enabled. If the front panel SYNC switch is depressed, data bit D0 will be logic 1. This data bit level commands the CPU to store the frequency data held in the selected vfo register into the other vfo register, giving both vfo registers the same frequency value.

When CS3R is logic 0, buffer U5 and part of buffer U6 are enabled. This permits data from a remote keypad to be input to the data bus. Two data bits are generated in parallel when any key on the keypad is depressed. One bit represents the keypad row and the other the column of the key.

At certain times data on the data bus is strobed into latching flip-flops for output to other circuit cards. Strobe signals are the CS2W, CS3W, CS5W, and CS6W outputs from decoders U3 and U4. Bits D0 through D7 are strobed into latches U11A and U11B when the inverted CS5W signal from U10D-8 goes from logic 0 to logic 1. This data remains at the flip-flop

outputs until the next CS5W positive-going transition strobes the then-present data bits to the outputs. The outputs are applied to the frequency display circuits card and to U12A, U12B, and U16. Data at J1-3, -5, -7 and -9 are binary coded for developing a decimal digit at the display. Data bits at J1-6, -8, and -10 are binary coded for addressing display decoders. These decoders steer the decimal digit to the correct display driver for that digit.

The U11 outputs are also applied to U12A, U12B, and U16 to be decoded and applied (from J4-11 through -17) to the remote device connector. Decoder U16 develops the strobe signals for U12A and U12B. When U16-10 and -13 are both logic 0, the output at U16-3 is logic 1 and that at U16-14 logic 1. When U16-10 goes to logic 1, U16-3 becomes logic 0 and U16-14 logic 1. For all other input combinations, both outputs are logic 0. As the outputs go from logic 0 to logic 1, the related latch, U12A or U12B, has data at the latch inputs strobed to the outputs and held until the next positive-going strobe transition. The resulting latch outputs are strobe and bcd operating-frequency signals for 10's-MHz and 1's-MHz digits.

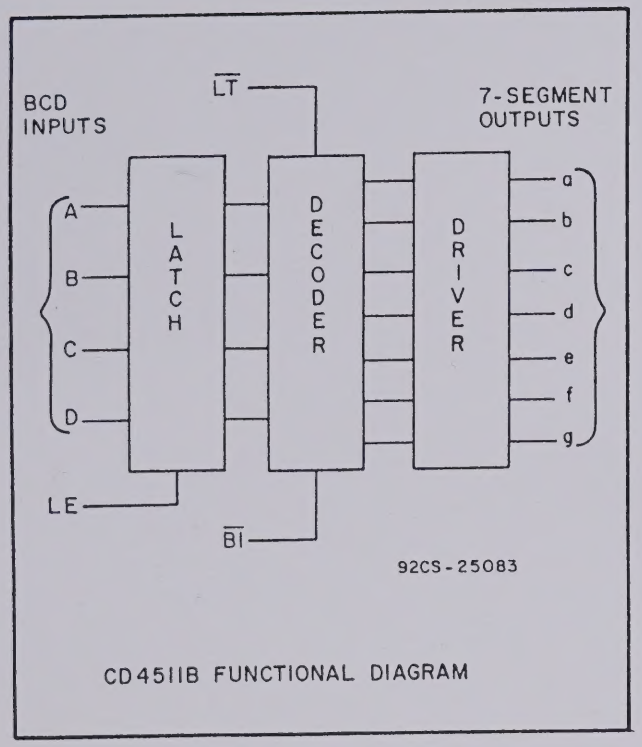
Data from the data bus is strobed into latches U14A and U14B when the inverted CS2W signal (from U10-10) goes from logic 0 to logic 1. At the same time, the CS3W signal goes from logic 0 to logic 1. Data bits D1, D2, D3 and D7, present when the CS3W signal is logic 1, are clocked into U13. The output from U13 and U14 develop: a low-pass filter selection signal, a band signal (B6, B8, or B9, for high-pass filter selection in the receiver), and a transmit inhibit signal. Data bits D5, D6, and D7 are clocked into latch U15 when the CS6W signal is logic 1. This data is output to the synthesizer circuit card as frequency data, clock, and strobe signals.

The transmit inhibit signal (CTTL) from U13 is logic 1 if the operating frequency is not within a band authorized for use by the Amateur Radio Service. The logic 1 filter select signals from U14A, U14B, and U13 turns on one of the five switching transistors (Q1 - Q5). The enabled transistor causes relays in the low-pass filter assembly to energize, selecting a particular filter. If low-pass filter assembly A2A3 is not installed, filters for the 2-3-MHz, 4-5-MHz, 5- through 7-MHz, and 10- through 14-MHz bands are not present. Diodes CR3, CR6, CR7, and CR9 perform an OR function to cause the next higher frequency band filter to be enabled on the A2A2 assembly if a frequency within the ranges covered by A2A3 is selected.

7.4 A10 DISPLAY BOARD THEORY

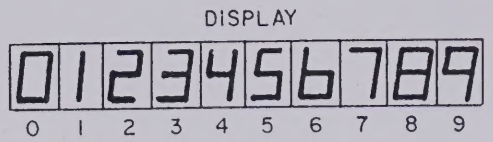
Refer to figure 7-6 and to the A10, display board, schematic. The display board takes address and frequency information from the control card and converts it to drive the front panel frequency readouts.

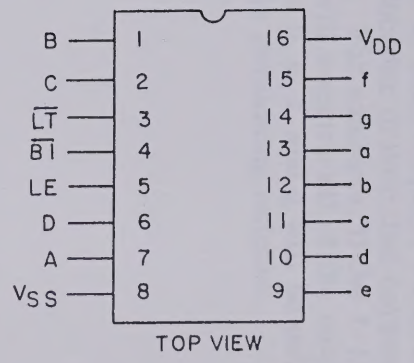
The frequency information is input to A10 at J1 pins 4, 6, 8, and 10, and applied to U2-U8. The address information enters A10 at J1, pins 5, 7, and 9, and is applied to U1, a three-line to eight-line decoder. At the output of U1, one of the seven outputs will be at logic 0 while the other six are at logic 1 for each address. If the 10 MHz frequency information is being input the 10 MHz address will also be present to produce a logic 0 at U1 pin 15 and logic 1's at pins 9 through 14. The logic 0 at pin 15 is applied to the lamp enable (LE) input of U2, pin 5. The logic 0 at pin 5 enables U2 and the four-line, 10-MHz, frequency information at pins 1, 2, 6, and 7 is converted to 7-segment information. The 7-segment information at U2, pins 9 through 4, drives the 10-MHz section of display DS1. With the 1-MHz frequency information being input, U1, pin 15, will be logic 1 and pin 14 will be logic 0 to enable the 1 MHz section of DS1.



CD4511B FUNCTIONAL DIAGRAM

COS/MOS BCD-TO-SEVEN-SEGMENT LATCH DECODER DRIVER





CD4511B TERMINAL ASSIGNMENT

Figure 7-6. CD4511B COS/MOX BCD-to-Seven Segment Latch Decoder Driver.

The outputs of the decoder drivers, U2 through U8, are labled a through f. These outputs correspond to the 7-segments in each display, which are also labled a through f. To display a number the outputs of the decoder driver that correspond to the segments that must be lit in the display will be logic 1. For example, if the 1-MHz frequency is 8, all 7 segments of the display must be on, this will require all of the output of U3 to be logic 1. If the 1-MHz frequency is 4, only segments b, c, f, and g will be on, requiring logic 1's at U3, pins 12, 11, 15, and 14, and logic 0's at the remaining outputs.

7.5 SELF-TEST

1. The frequency at A8U2, pin 39 is _____ MHz.

2. Data is read into the CPU when the read/write (R/W) line is at logic _____.

3. Information from the front panel frequency control switches, A8J6 pins 7 through 10, is transferred through U6 when U6, pin 1 is at logic _____.

4. The input to control card A8, from the front panel tuning knob, enters A8 at J6 pins _____ and _____.

5. Frequency information used in the front panel frequency readout is from A8J1 pin _____ and pins _____ through _____.

6. With a transmit operating frequency of 1.95000 MHz the low-pass filter outputs of A8 will be:

   A8J2 pin 6 = logic _____

   A8J2 pin 7 = logic _____

   A8J2 pin 8 = logic _____

   A8J2 pin 9 = logic _____

   A8J2 pin 10 = logic _____

7.6 SELF-TEST ANSWERS

1. 3.3 MHz
2. logic 1
3. logic 0
4. pins 1 and 2
5. pin 3 and pins 5 through 10
6. pin 6 = logic 0

   pin 7 = logic 1

   pin 8 = logic 1

   pin 9 = logic 1

   pin 10 = logic 1

Section 8

Final Examination

This section includes the final examination on the KWM-380 Transceiver. In order to qualify for a certificate of completion, you must answer all the questions to the best of your knowledge and submit the examination for grading to the Training Department of the Collins Telecommunications Products Division of Rockwell International. Mail your answers to:

Collins Telecommunications Products Division
Rockwell International
Customer Training 179-400
855 - 35th St. N.E.
Cedar Rapids, IA 52406

KWM-380 FINAL EXAMINATION

1. The voltage applied to A2A2J3, pin 7, is _____V during receive operation.

2. The operating _____ determines which of the high-pass filters in receiver-exciter card A3 is enabled.

3. To reduce the rf signal level at the junction of CR103 and CR107, the forward bias applie to pin diode A3CR104 must _____.

4. The injection frequency applied to A3U100, pin 8, can range from _____ to _____ MHz.

5. What is the frequency of the injection to A3U100, pin 8, with a receive operating frequency of 15.000 00 MHz? _____

6. During receive operation the output of the first receive mixer is routed through broadband amplifier Q100 by forward biased diodes CR _____ and CR_____.

7. What is the phase relationship of the receive signal on the source and drain of U100?
_____

8. Crystal filter A3, FL1A/B has a bandpass of_____ kHz.

9. As received signal strength increases, the AGC voltage at Q102, must _____ to maintain a constant amplitude audio output from the receiver.

10. With a receive operating frequency of 7.649 00 MHz, the injection to the second receive mixer, U101, pin 8, is_____ MHz.

11. The received sideband, upper or lower, is determined by which front panel control?
_____

12. The front panel PBT control is enabled in receive by a logic 1 input to the passband tuning circuit at A3J1, pin _____.

13. A13R65 on the source of mixer Q1 adjusts the _____ of the amplifier.

14. In AM operation the nominal output frequency from the passband tuning circuit at A13J(is _____ MHz.

15. The output of the passband tuning circuit is blocked from mixer A3U103 by _____ in receive operation.

16. To reduce the gain of the receiver, the AGC voltage applied to the anode of CR700 must _____.

17. What is the function of variable resistor R702 on the input of if amplifier A3U700?

_____

18. During CW, receive operation the input at pin 2 of product detector A3U701 is _____ kH

19. What is the injection frequency applied to A3U701, pin 2, during sideband, receive operation? _____ kHz.

20. With loss-of-lock in the synthesizer, during receive operation, the signal at A3U601D, pin 13, will be _____

21. During CW, transmit operation the 455-kHz is injected into the signal path through CR_____, CR_____, CR_____ and Q_____ on the A3 board.

22. In A4, the passband tuning circuit, J1, pin 13, will be a logic 1 when transmitting in which mode? _____

23. With a transmit operating frequency of 14.000 00 MHz the injection to the first transmi mixer, A3U103, pin 8, is _____ MHz.

24. What is the purpose of transistor switch A3Q107?_____

_____

25. The 39.145-MHz transmit if signal is routed through A3Q101, by forward biasing CR_____ and CR_____, and reverse biasing CR_____ and CR_____.

26. The variable injection frequency to the second transmit mixer, A3U100, pin 8, is_____ _____ MHz with a transmit frequency of 14.000 00 MHz.

27. During transmit operation A3CR105 is forward biased by the +9-V dc xmt to provide

_____

_____

28. CR200 in the exciter broadband amplifier provides _____ for Q204 during transmit operation.

29. If, during transmit operation, the ALC voltage applied to the anode of CR2 in the PA (A1A1) increases sufficiently to forward bias Q1, the voltage at the emitter of Q4 will _____ to lower the pa rf output.

30. As A1A1R63 is adjusted to increase the voltage at pin of U101B the idle current of the output stage will _____.

31. A logic _____ at A1J3, pin 17 ($\overline{\text{AVG ALC INHIBIT}}$), disables the average power amplifier.

32. In the pa ALC thermal limiting circuit, as the temperature of RT101 increases the output of U101C, pin 8 _____.

33. Transmit monitor (XMT MONITOR) A1J3 pin 6, is a logic 0 when pa output power is greater than _____ watts.

34. Adjusting A9A1R23 will cause the output voltage of the _____ V regulator to vary.

35. Adjusting A9A1R14 ccw will _____ the output voltage of U3.

36. One purpose of A9VR2 is to provide _____.

37. A9A2Q1 is switched on and off by U1 at a _____ kHz rate.

38. The output of the switching regulator is regulated at +24 V by _____.

39. In the noise blanker A11, the output of oscillator Q3 must be _____ V rms or greater.

40. To block a noise pulse monostable multivibrator A11U3 produces a logic 0 pulse of _____ _____ μs duration at pin 11.

41. As the receive signal input to A11P1 increases, the AGC applied to U1, pin 5, will _____ to maintain a constant output amplitude from the detector.

42. The gain from the input of A11P1, to the output, P2, is _____ dB.

43. When the audio speech processor, A12, is enabled, U12A, pin 13, is logic _____, U12B, pin 5, is logic _____ and U12C, pin 6, is logic _____.

44. The bandpass of active audio filter U1A and U1B, A12, is _____ to _____ Hz.

45. The phase difference between the signals at A12TP1 and TP2 is _____ degrees.

46. The amplitude of the output signal from A12 is controlled by variable resistor R _____.

47. In loop 1 of the synthesizer (A5) the output of U1 pin 11 can range from _____ to _____ MHz.

48. Changing the operating frequency of the transceiver by 10 Hz will produce a _____-Hz frequency change at A5U1, pin 11.

49. With the synthesizer locked the output of U12B, pin 8, in loop 2 will be _____ kHz

50. With a dial frequency of 117.5000 00 MHz, the outputs of U18 are:
    pin 7 = logic _____
    pin 14 = logic _____
    pin 13 = logic _____
    pin 12 = logic _____
    pin 11 = logic _____

51. If the loop 2 VCO is operating at 47.2 MHz, the division ratio of the loop 2 variable divider is _____.

52. A logic 0 at A5J1, pin 9, indicates that the synthesizer is _____.

53. The frequency range of the variable reference frequency loop VCO is _____ to _____ MHz.

54. The division range of the variable reference frequency loop variable divider is _____ to _____.

55. With a dial frequency of 13.68499 MHz, the outputs of U21, U22, and U23 are:
    U23 pin 7 = logic _____
    U23 pin 14 = logic _____
    U23 pin 13 = logic _____
    U23 pin 12 = logic _____
    U23 pin 11 = logic _____
    U22 pin 4 = logic _____
    U22 pin 5 = logic _____
    U22 pin 6 = logic _____
    U22 pin 7 = logic _____
    U22 pin 14 = logic _____
    U22 pin 13 = logic _____
    U22 pin 12 = logic _____
    U22 pin 11 = logic _____
    U21 pin 4 = logic _____
    U21 pin 5 = logic _____
    U21 pin 6 = logic _____
    U21 pin 7 = logic _____

U21 pin 14 = logic _____

U21 pin 13 = logic _____

U21 pin 12 = logic _____

U21 pin 11 = logic _____

56. The output of A5U5B, pin 13, is a _____Hz signal.

57. A logic _____ at A5J1, pin 6, indicates a fault in the synthesizer.

58. With a 3.3-MHz input to A8U2, pin 39, the output Ø2 at pin 37 is a _____ kHz signal.

59. VFO SELECT information at A8J6, pin 3, is transferred through U7 to the data bus when U7, pin 1, is at logic _____.

60. Bcd frequency information used in the front panel frequency display is output from A8 at J1 pins _____, _____, _____, and _____.

61. With an operating frequency of 7.000 00 MHz the low-pass filter control outputs are:

A8J2 pin 6 = logic _____

A8J2 pin 7 = logic _____

A8J2 pin 8 = logic _____

A8J2 pin 9 = logic _____

A8J2 pin 10 = logic _____

62. The serial frequency data used in the synthesizer is output from control board at A8J3 pin _____.

NAME _____

DATE _____

ADDRESS _____

_____

_____

COMPANY _____

9.1 OBJECTIVES

9.2 INTRODUCTION TO SINGLE SIDEBAND

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Figure 9-2.3
Figure 9-2.4
Figure 9-2.5
Figure 9-2.6
Figure 9-2.7
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9.3 BASIC LOGIC SYMBOLS AND TRUTH TABLES

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9.4 LM555, TIMER

Figure 9-4.1

9.5 74LS191, 4-BIT BINARY UP/DOWN-COUNTER

Figure 9-5.1
Figure 9-5.2

9.6 CD4066 SWITCH

Figure 9-6.1

9.7 SRA-1 DOUBLE BALANCED MIXER

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9.8 CA3028 PRODUCT DETECTOR

Figure 9-8.1

9.9 μA757 GAIN CONTROLLED IF AMPLIFIER

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9.10 VOLTAGE VARIABLE CAPACITOR

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9.11 PIN IN5767, DIODE CHARACTERISTICS

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9.12 OPERATIONAL AMPLIFIERS

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9.13 OPERATIONAL AMPLIFIER CIRCUIT APPLICATIONS

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9.14 FIELD EFFECT TRANSISTORS

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9.15 DUAL-GATE FET APPLICATIONS

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9.16 TRANSISTOR STAGE TROUBLESHOOTING

Figure 9-16.1
Figure 9-16.2

9.17 COMPUTER AND INTEGRATED-CIRCUIT GLOSSARY

9.1 OBJECTIVES

This section of the self-study manual provides reference information to assist the student in understanding the operation of circuits within the KWM-380 and assist in troubleshooting circuits when a failure occurs.

9.2 INTRODUCTION TO SINGLE-SIDEBAND

Single-sideband (SSB) communication is a method whereby the rf carrier and one sideband of an amplitude modulated wave are suppressed. Single-sideband communication possesses certain advantages over AM communication.

Some of the advantages are:

a. Relative immunity to the effects of selective fading.
b. To produce the same received signal-to-noise ratio, 9 dB, an AM transmitter must produce three times more power at the antenna.
c. More efficient utilization of the limited hf spectrum. Maximum authorized bandwidth in the hf spectrum is 12 kHz. SB requires a 3-kHz bandwidth.

Figure 9-2.1 illustrates the spectrum occupied by a 3900-kHz AM and SSB signal, each modulated by a single 1-kHz tone. The AM signal consists of a carrier and two sidebands containing identical intelligence. The SSB signal on the other hand is made up of a single sideband containing essentially all the transmitted power and the same intelligence as the AM wave.

The operation of the SSB receiver is basically the reverse process used in SSB transmission. The received SSB signal is amplified, translated downward in frequency to one or more

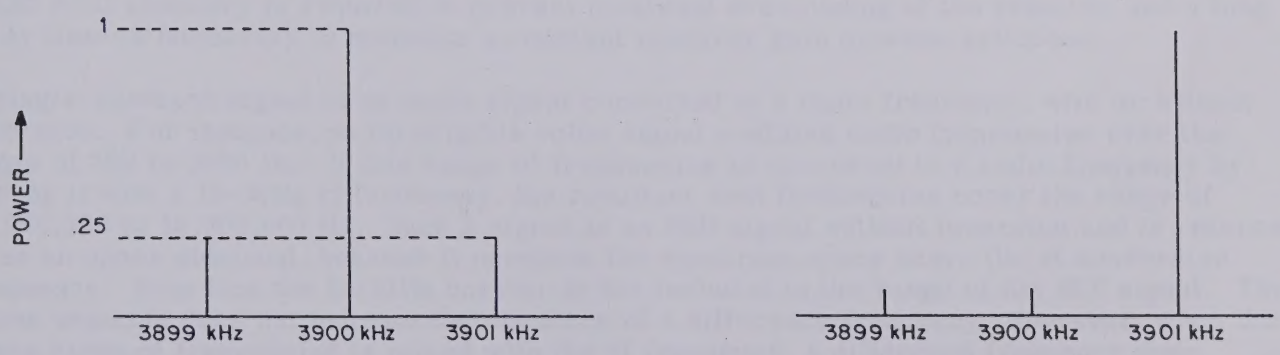


Figure 9-2.1. Comparison of AM and SSB Spectra.

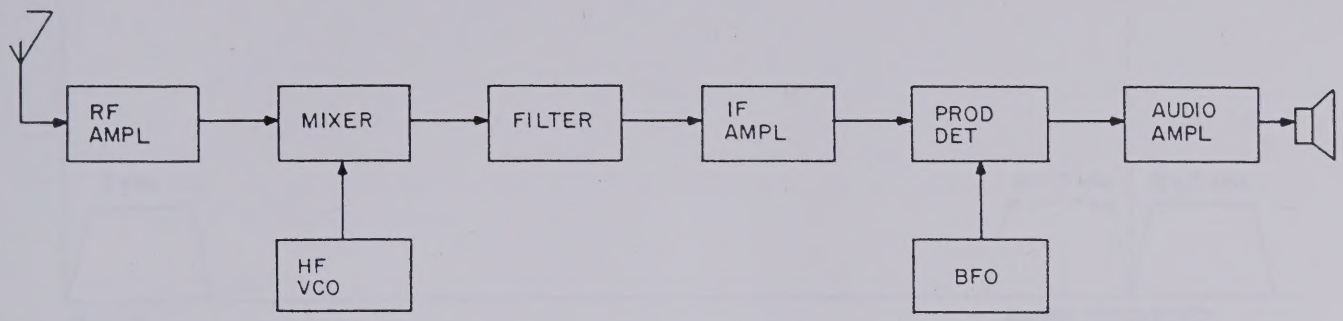


Figure 9-2.2. SSB Receiver Simplified Block Diagram.

intermediate frequencies where the signal receives further amplification, and converted back to the original frequencies by a product detector. This operation is basically a process of frequency translation. The block diagram of figure 9-2.2 illustrates a SSB receiver.

To take full advantage of the narrow bandwidth occupied by a SSB signal, selectivity characteristics in the receiver must be controlled carefully. Any excess in receiver bandwidth over that required to pass the desired signal causes degradation of the signal by passing unnecessary interference and noise.

An AM envelope amplitude detector circuit can be used to detect a SSB signal, with local carrier supplied by a bfo. The amplitude of the bfo injection signal must be several times greater than that of the receive signal at the detector to minimize distortion. Much lower distortion figures are available if product detectors are used for SSB demodulation. The product detector translates the receive if signal to audio by mixing it with a locally generated carrier signal.

Still another difference between the AM and SSB receiver is the AGC attack time. The AM AGC is derived from the received carrier signal level. Since the carrier level normally does not vary with modulation, AGC voltage stays fairly constant, so that the attack of the AM AGC system is not a highly important consideration. In contrast, the signal level in an SSB receiver varies over a wide range of syllabic rate, therefore a fast attack characteristic in the AGC circuitry is required to prevent continual overloading of the receiver and a long delay time is necessary to maintain a constant receiver gain between syllables.

A single-sideband signal is an audio signal converted to a radio frequency, with or without inversion. For instance, an intelligible voice signal contains audio frequencies over the range of 300 to 3000 Hz. If this range of frequencies is converted to a radio frequency by mixing it with a 15-MHz rf frequency, the resultant sum frequencies cover the range of 15,000,300 to 15,003,000 Hz. Such a signal is an SSB signal without inversion and is referred to as an upper sideband, because it occupies the spectrum space above the rf conversion frequency. Note that the 15-MHz carrier is not included in the range of the SSB signal. The above example does not indicate the presence of a difference frequency. However, when the same range of frequencies is mixed with the rf frequency, a difference frequency does develop which covers the range from 14,999,700 to 14,997.000 Hz. This signal is also an SSB signal but with inversion. This SSB signal is referred to as a lower-sideband signal because occupies the spectrum space below the rf conversion frequency. Lower-sideband is

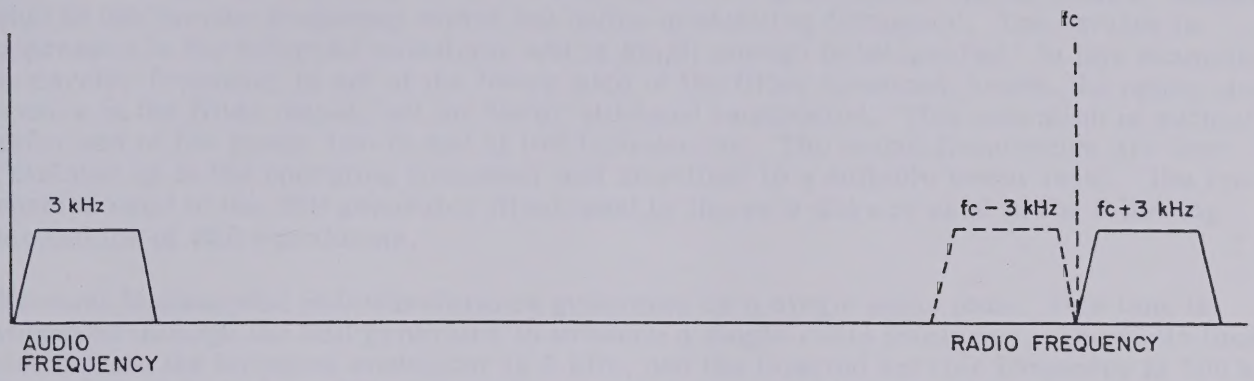


Figure 9-2.3. Location of SSB Signal in RF Spectrum.

seldom used except for amateur and some specialized military work. Figure 9-2.3 illustrates the position of the SSB signal in the rf spectrum.

From the above description of the SSB signal, it is apparent that only one sideband signal need be transmitted to convey the intelligence. Since two sideband signals are obtained from the mixing process, it is also necessary to remove one sideband before transmission. To receive the SSB signal it is necessary to convert the SSB signal back to the original audio signal. This requires identical transmitter and receiver conversion frequencies.

There are two methods for generating SSB signals. One method utilizes phasing of signal components to suppress the unwanted sideband. This method is outmoded and therefore will not be discussed in this manual. The method that will be covered employs a filter which rejects one sideband. This method is used in the KWM-380. As shown in figure 9-2.4, a typical filter type SSB generator consists of a balanced modulator followed by a filter with suitable selectivity characteristics to pass one sideband and reject the other.

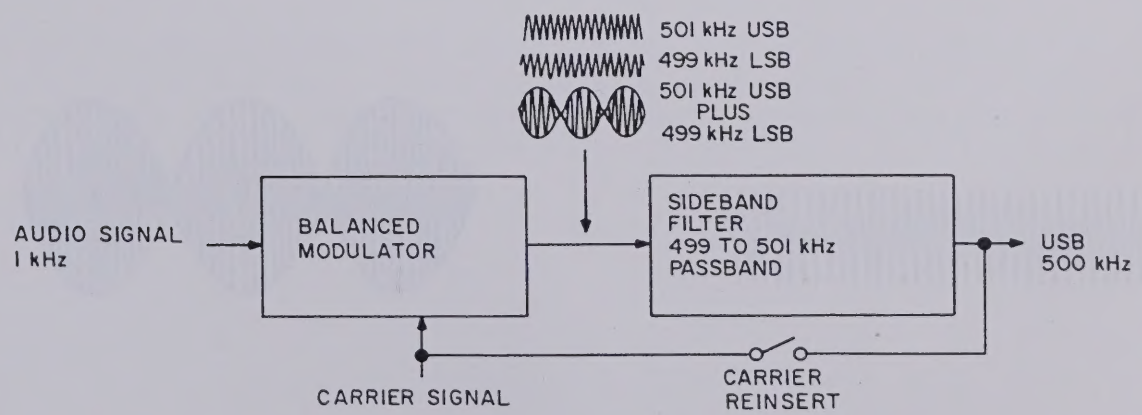


Figure 9-2.4. Filter-Type SSB Generator.

The balanced modulator produces basically two output frequencies: (1) an upper sideband equal to the carrier frequency plus the audio-modulating frequency and (2) a lower sideban equal to the carrier frequency minus the audio-modulating frequency. The carrier is suppressed in the balanced modulator and is small enough to be ignored. In this example, the carrier frequency is set at the lower edge of the filter passband; hence, the upper sideb appears at the filter output, but the lower sideband is rejected. This operation is normally performed at low power levels and at low frequencies. The output frequencies are then translated up to the operating frequency and amplified to a suitable power level. The frequencies used in the SSB generator illustrated in figure 9-2.4 are used in the following discussions of SSB waveforms.

The most fundamental SSB waveform is generated by a single audio tone. This tone is processed through the SSB generator to produce a single radio frequency. The audio tone injected into the balanced modulator is 1 kHz, and the injected carrier frequency is 500 kH The output of the balanced modulator consists of a lower sideband at 499 kHz and an upper sideband at 501 kHz. These two sidebands, being of equal amplitude, produce the characte istic half sine-wave envelope shown in figure 9-2.5. The repetition rate of this envelope is 2 kHz, the difference between the frequencies represented by the envelope. This rf signal, containing both upper and lower sidebands, is a double sideband (DSB) signal.

By passing the DSB signal through a filter with a passband of 500.3 kHz to 502.7 kHz, the upper sideband is passed while the lower sideband is attenuated. The output signal from th generator is a single radio frequency as shown in figure 9-2.6.

In the KWM-380, the lower sideband is removed when the passband tuning oscillator freque is 6.711500 MHz.

From the single-tone SSB signal without carrier, it is a simple step to generate the single-tone SSB signal with carrier. This is done by reinserting the carrier after the filtering operation as shown in figure 9-2.4. When the reinserted carrier has the same amplitude a the SSB signal, the resulting waveform is like the DSB waveform shown in figure 9-2.5. However, the frequency components of the two waveforms are not the same. The frequency components of the SSB signal with carrier are 501 kHz (upper sideband) and 500 kHz (carri The SSB signal with full carrier can be demodulated with a conventional diode detector use in AM receivers without serious distortion or loss of intelligibility.

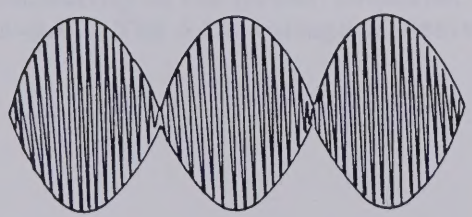


Figure 9-2.5. Single-Tone DBS or Two-Tone SSB Waveform.

Figure 9-2.6. Single-Tone SSB Waveforn

If the amplitude of the reinserted carrier is less than that of the single-tone SSB signal, the waveform shown in figure 9-2.7 results. This waveform is typical in systems using a pilot carrier and is the same when the single tone SSB signal is less than the carrier which is the same in the AM equivalent mode (AME). To demodulate the signal properly, the carrier must be reinforced at the receiver to a level not less than the amplitude of the sideband signal. The receiver bfo can be used as the source of additional carrier energy required to demodulate such a signal, but more sophisticated methods are used for commercial applications.

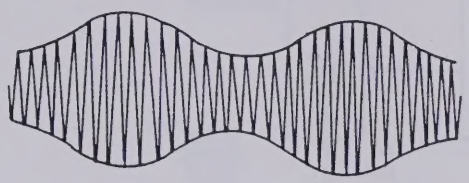
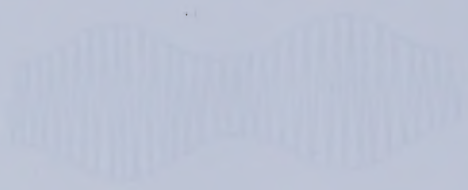


Figure 9-2.7. Single-Tone SSB Waveform with Pilot Carrier.

Overall transmission efficiency depends upon the average power transmitted, while transmitter power is limited to the peak capability of the transmitter. For voice transmission, it is therefore desirable to use speech processing circuits which will increase the average power in the voice signal without increasing peak power. This is normally done with a speech compressor circuit.

A speech compressor is an automatic variable gain amplifier which maintains a relatively constant output level to compensate for variations in voice levels at the microphone thus maintaining optimum transmitter modulation.

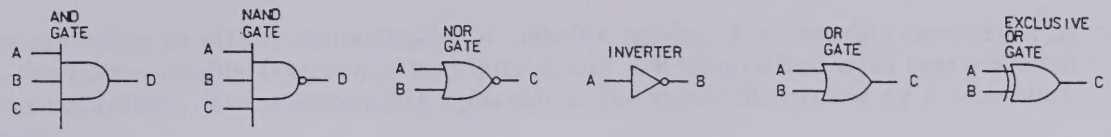
The transmitter gain is maintained at the highest usable level without exceeding the peak-power capability of the power amplifier by the automatic load control (ALC) circuit (refer to figure 9-2.8). The ALC voltage is derived from the SSB envelope rather than an audio input signal.



SPEECH COMPRESSOR
AUDIO AMPL
BALANCED MOD
CARRIER GEN
SIDEBAND FILTER
MIXER
HIGH-FREQ RF OSC
LINEAR RF AMPL
ALC
f_A (AUDIO)
F_C
$F_C \pm F_A$
F_C (CARRIER)
$F_C \pm F_A$
F_{OPR} (USB)

9.3 BASIC LOGIC SYMBOLS AND TRUTH TABLES (Refer to figure 9-3.1.)

BASIC LOGIC SYMBOLS



D = ABC

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

D = $\overline{ABC}$

A	B	C	D
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

C = $\overline{A+B}$

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

B = $\bar{A}$

A	B
1	0
0	1

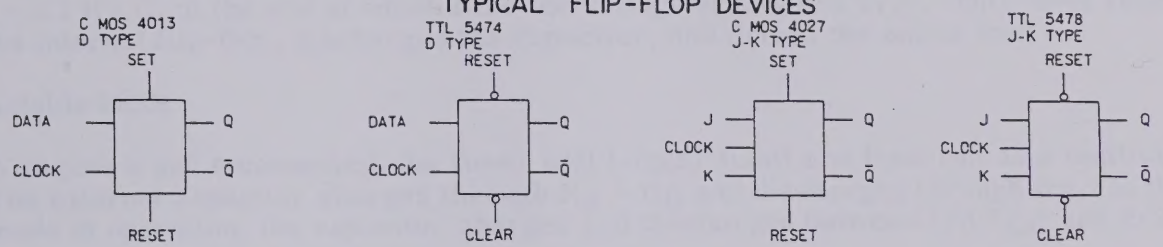
C = A+B

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

C = $A\bar{B} + \bar{A}B$

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0

TYPICAL FLIP-FLOP DEVICES



C MOS 4013

INPUTS				OUTPUTS	
CLOCK	DATA	RESET	SET	Q	$\bar{Q}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
⌐	X	0	0	Q_0	$\bar{Q}_0$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

④ TTL 5474

INPUTS				OUTPUTS	
CLOCK	DATA	CLEAR	RESET	Q	$\bar{Q}$
⌐	1	1	1	1	0
⌐	0	1	1	0	1
⌐	X	1	1	Q_0	$\bar{Q}_0$
X	X	1	0	1	0
X	X	0	1	0	1
X	X	0	0	1*	1*

* NONSTABLE, WILL NOT STAY WHEN PRESET AND CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.

C MOS 4027

INPUTS						OUTPUTS	
CLOCK	J	K	S	R	Q_0	Q	$\bar{Q}$
⌐	1	X	0	0	0	1	0
⌐	X	0	0	0	1	1	0
⌐	0	X	0	0	0	0	1
⌐	X	1	0	0	1	0	1
⌐	X	X	0	0	X	Q_0	$\bar{Q}_0$
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

TTL 5478

INPUTS					OUTPUTS	
CLOCK	J	K	P	CLEAR	Q	$\bar{Q}$
⌐	0	0	1	1	Q_0	$\bar{Q}_0$
⌐	1	0	1	1	1	0
⌐	0	1	1	1	0	1
⌐	1	1	1	1	TOGGLE	
X	X	X	0	1	1	0
X	X	X	1	0	0	1
X	X	X	0	0	1*	1*

* NONSTABLE, WILL NOT STAY WHEN PRESET AND CLEAR INPUTS RETURN TO THEIR INACTIVE (HIGH) LEVEL.

NOTES:

① FLIP FLOP DEVICES SHOWN ARE POSITIVE EDGE TRIGGERED DEVICES.

② 1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE.

③ Q_0=Q STATE BEFORE CLOCK TRANSITION.

④ POSITIVE LOGIC - LOW INPUT TO PRESET SETS Q TO HIGH LEVEL, LOW INPUT TO CLEAR SETS Q TO LOW LEVEL. PRESET AND CLEAR ARE INDEPENDENT OF CLOCK.

TP5-3436-014

Figure 9-3.1. Basic Logic Symbols and Truth Tables.

9.4 LM555, TIMER

9.4.1 Description

This device operates in either monostable or astable mode. For astable operation as an oscillator, the free-running frequency and duty cycle are controlled with two external resistors and one capacitor. For monostable operation, the timer functions as a one-shot multivibrator.

9.4.2 Applications

a. Monostable Mode

The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, an internal flip-flop is set which both releases the short circuit across the capacitor and drives the output high. The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. This level resets the internal flip-flop, discharges the capacitor, and drives the output low.

b. Astable Mode

With pins 2 and 6 connected, the timer will trigger itself and free-run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. Refer to figure 9-4.1.

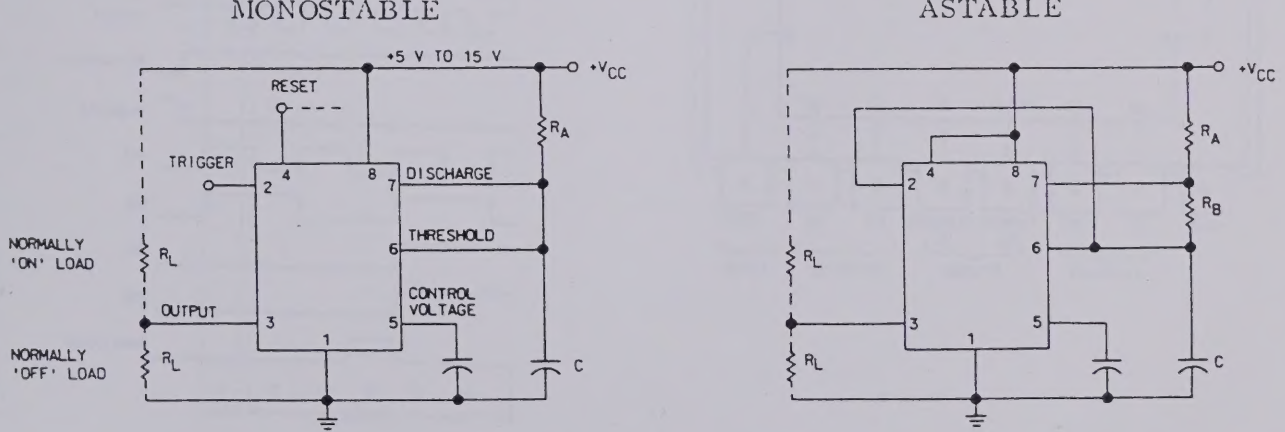


Figure 9-4.1. LM 555 Timer Diagram.

9.5 74LS191, 4-BIT BINARY UP/DOWN-COUNTER

9.5.1 Description

This device is a synchronous, reversible, 4-bit binary up/down-counter. Synchronous operation is provided by having all flip-flops clocked simultaneously. The outputs are triggered on a low-to-high transition of the clock with enable low. The count direction is determined by the level of the up/down input. When low, the counter counts up and when high, it counts down. The counter is fully programmable. The average propagation delay is 20 ns. V_{CC} is +5 V dc nominally.

9.5.2 Logic

The typical load and count sequence table is shown in figure 9-5.1.

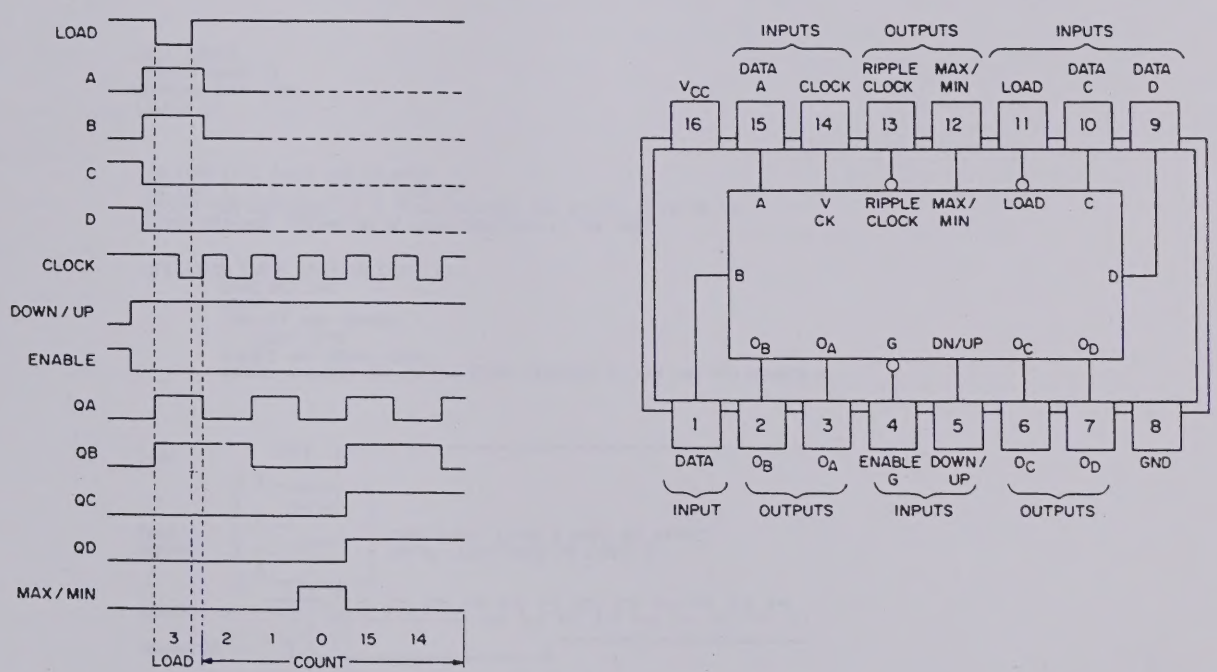
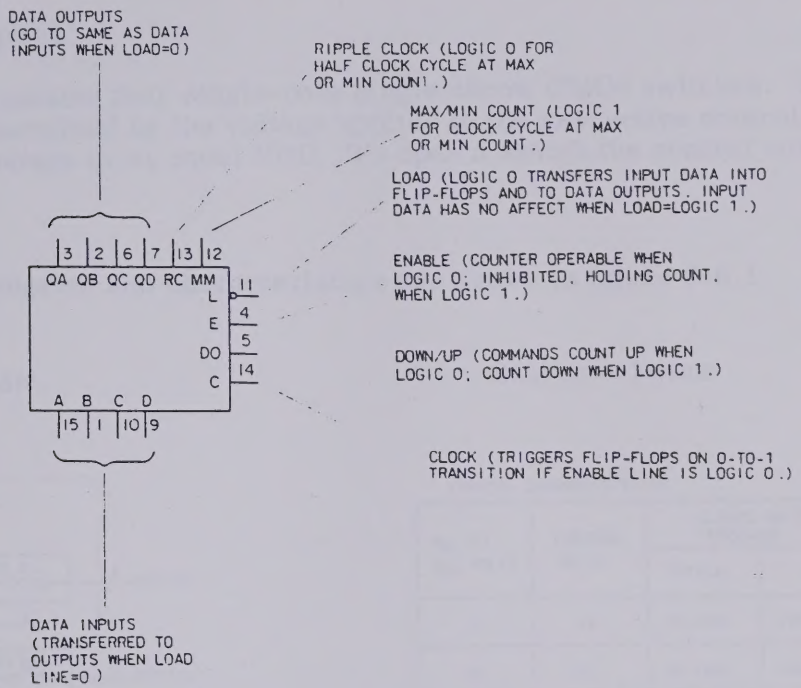


Figure 9-5.1. 74LS191 Count Sequence and Connection Diagram.

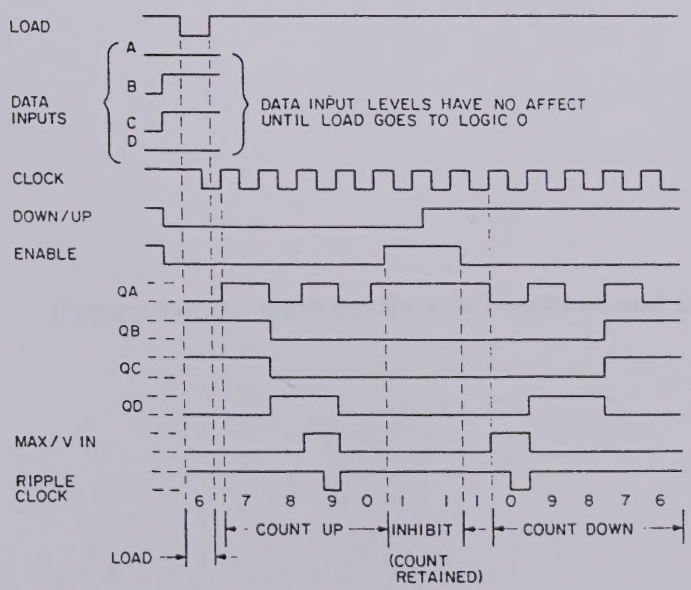
9.5.3 Programmable Divider Operation (Refer to figure 9-5.2.)


DATA OUTPUTS
(GO TO SAME AS DATA
INPUTS WHEN LOAD=0)
RIPPLE CLOCK (LOGIC 0 FOR
HALF CLOCK CYCLE AT MAX
OR MIN COUNT.)
MAX/MIN COUNT (LOGIC 1
FOR CLOCK CYCLE AT MAX
OR MIN COUNT.)
LOAD (LOGIC 0 TRANSFERS INPUT DATA INTO
FLIP-FLOPS AND TO DATA OUTPUTS. INPUT
DATA HAS NO AFFECT WHEN LOAD=LOGIC 1.)
ENABLE (COUNTER OPERABLE WHEN
LOGIC 0; INHIBITED, HOLDING COUNT,
WHEN LOGIC 1.)
DOWN/UP (COMMANDS COUNT UP WHEN
LOGIC 0; COUNT DOWN WHEN LOGIC 1.)
CLOCK (TRIGGERS FLIP-FLOPS ON 0-TO-1
TRANSITION IF ENABLE LINE IS LOGIC 0.)
3 2 6 7 13 12
QA QB QC QD RC MM
L 11
E 4
DO 5
C 14
A B C D
15 1 10 9
DATA INPUTS
(TRANSFERRED TO
OUTPUTS WHEN LOAD
LINE=0)

74LS190 IS A 4-BIT BCD COUNTER.
74LS191 IS A 4-BIT BINARY COUNTER.
EXCEPT FOR BCD COUNT OF 9 BEING MAXIMUM AND BINARY COUNT OF 15
BEING MAXIMUM, OPERATION OF BOTH COUNTERS IS THE SAME.

OPERATION SHOWN (FOR 74LS19C) IS:
- LOAD BCD SIX
- COUNT UP
- INHIBIT AND COMMAND
  - COUNT DOWN
- ENABLE AND COUNT DOWN

(NOTE: MAX/MIN AND RIPPLE CLOCK OUTPUTS AT MAX AND MIN COUNTS.)



TPA-0835-014

Figure 9-5.2. Programmable Divider Counter Operation.

9.6 CD4066 SWITCH

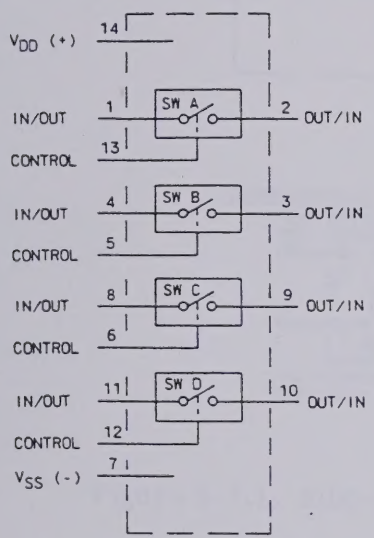
9.6.1 Description

This device contains four single-pole single-throw CMOS switches. The state of each switch section is determined by the voltage applied to the respective control input. To close a switch the control voltage must equal VDD. To open a switch the control voltage must equal VSS.

9.6.2 Logic

The switch diagram and characteristics are shown in figure 9-6.1.

Switch Diagram



Characteristics

TYPICAL CHARACTERISTICS

V_{DD} TO V_{SS} VOLTS	CONTROL VOLTS	CLOSED-SWITCH IMPEDANCE		TYPICAL OPEN-SWITCH IMPEDANCE
		TYPICAL	MAX	
15	15	60-145Ω	220-320Ω	10 kΩ
10	10	89-190Ω	400-550Ω	10 kΩ
5	5	160-360Ω	3000-5500Ω	10 kΩ

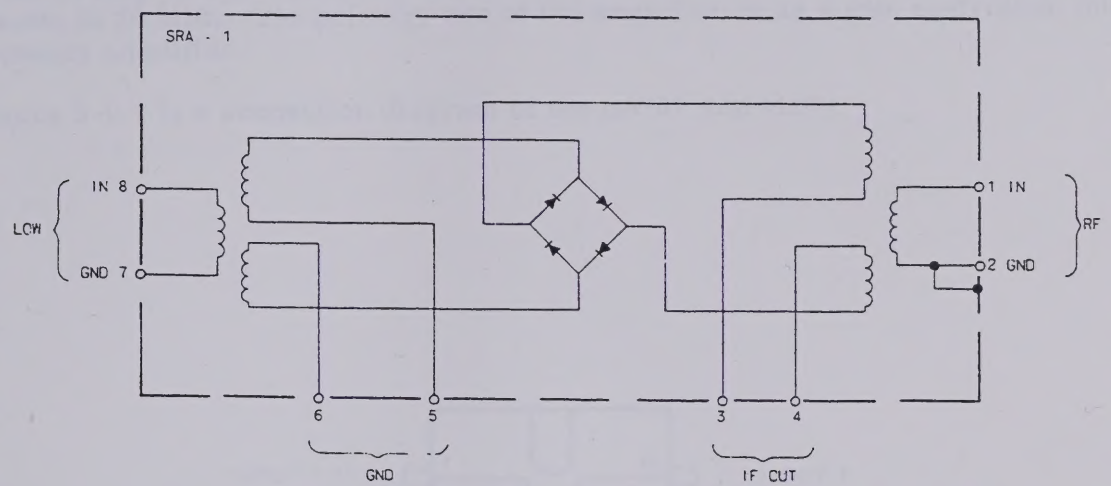
NOTE: CONTROL VOLTAGE MUST EQUAL V_{DD} TO CLOSE SWITCH.
CONTROL VOLTAGE MUST EQUAL V_{SS} TO OPEN SWITCH.

TP5-2283-013

Figure 9-6.1. CD4066 Switch Diagram and Characteristics.

9.7 SRA-1 DOUBLE BALANCED MIXER

9.7.1 Figure 9-7.1 shows a simplified schematic diagram, input-output terminals, and the characteristics of the SRA-1 double-balanced mixer.



CHARACTERISTICS

PEAK INPUT POWER: 50 mW MAX
PEAK CURRENT, ANY PORT: 40 mA MAX
FREQUENCY RANGE (MHz):
LOW - 0.5 TO 500
RF - 0.5 TO 500
IF - DC TO 500
CONVERSION LOSS: 6.5 dB TYPICAL,
8.5 dB MAX. (SIGNAL AT IF PORT,
OUTPUT AT RF PORT)
TEST CURRENT WHEN CHECKING
CONTINUITY MUST NOT EXCEED 20 mA.

ISOLATION (dB):
LOW BAND EDGE:
LOW TO RF - 35 dB MIN.
LOW TO IF - 30 dB MIN
MID-RANGE:
LOW TO RF - 30 dB MIN.
LOW TO IF - 25 dB MIN.
UPPER BAND EDGE:
LOW TO RF - 25 dB MIN
LOW TO IF - 20 dB MIN

TP5-2278-013

Figure 9-7.1. SRA-1 Double Balanced Mixer Simplified Schematic Diagram.

9.8 CA3028 PRODUCT DETECTOR

9.8.1 Figure 9-8.1 is a simplified schematic of a CA3028, differential/cascade amplifier, which is used as a product detector in the KWM-380.

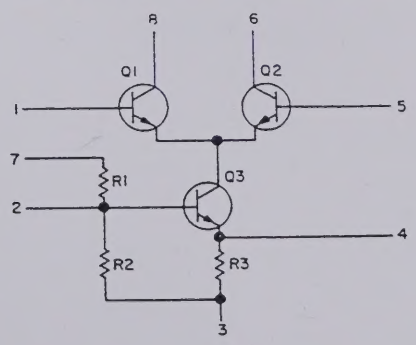


Figure 9-8.1. CA3028 Product Detector Simplified Schematic.

9.9 μA757 GAIN CONTROLLED IF AMPLIFIER

9.9.1 Description

The μA757 is a high-performance, gain controlled if amplifier. The amplifier contains two sections which may be used independently, or in cascade. The frequency range of the μA757 is from audio to 25 MHz. The primary use of the amplifier is as a gain controlled, intermediate frequency amplifier.

9.9.2 Figure 9-9.1 is a connection diagram of the μA757 (top view).

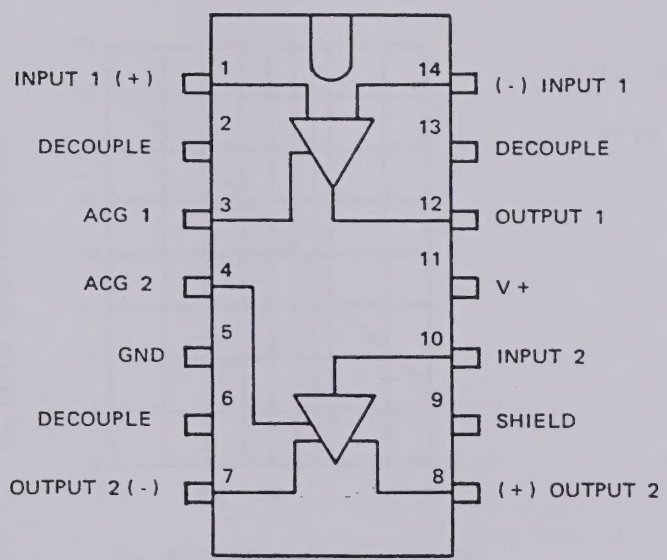


Figure 9-9.1. μA757 Connection Diagram.

9.10 VOLTAGE VARIABLE CAPACITOR

9.10.1 Description

Voltage variable capacitors are p-n junction diodes that behave as capacitors with a reasonable Q when biased in the reverse direction. The actual capacitance value, within the range of the diode, is determined by the dc bias voltage applied to it. In a typical voltage variable capacitor the capacitance can be varied over a 5- to 30-pF range with a bias change from 3 to 20-volts.

9.10.2 Reverse Voltage Vs Capacitance Chart is shown in figure 9-10.1.

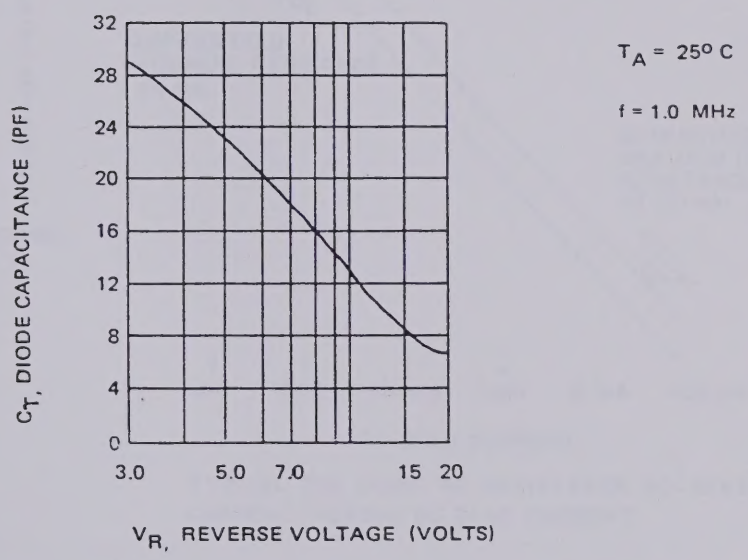


Figure 9-10.1. Voltage Variable Capacitor Reverse Voltage vs Capacitance Chart.

9.11 IN5767, PIN DIODE

9.11.1 Description

Pin diodes are p-n junction diodes in which the rf resistance is inversely proportional to the amount of dc forward bias current. As the dc bias current through the diode increases the rf resistance decreases.

9.11.2 Figure 9-11.1 shows the typical rf resistance slope distribution for a IN5767 diode.

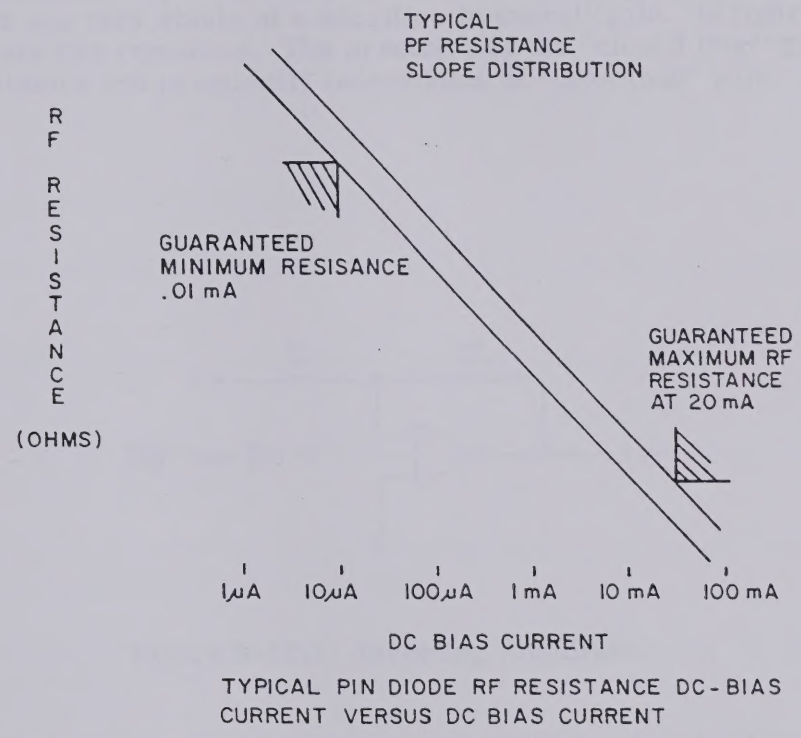


Figure 9-11.1. IN5767 Pin Diode Typical RF Resistance Slope Distribution.

9.12 OPERATIONAL AMPLIFIERS

9.12.1 Description

Operational amplifiers were originally designed for use in analog computers to perform various mathematical operations. It was found that the application of negative feedback around a high gain dc amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of feedback components, operational amplifier circuits could be used to add, subtract, average, integrate, and differentiate.

Gain Adjustment

The gain of the operational amplifier is a direct result of the use of negative feedback. The gain characteristics are very stable at a sacrifice in overall gain. In figure 9-12.1, the feedback elements are two resistors. The precision of the "closed loop" gain is set by the ratio of the two resistors and practically independent of "open loop" gain.

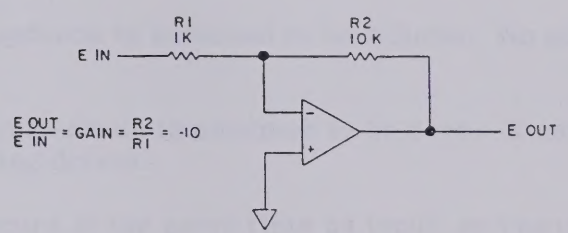


Figure 9-12.1. Inverting Amplifier.

Figure 9-12.1 operational amplifier has two input terminals. One is inverting and is labeled -; the other is noninverting and is labeled +. In the configuration used, the output is inverted from the input and amplified x 10. Hence, the notation used in -10. If a different gain is desired, different R1, R2 resistors are selected.

Input Terminals

Due to the high gain the amplifier possesses, the voltage measured at the inverting input will be extremely small. So small in fact, that it can be assumed to be ground, - - a "virtual ground." This allows connecting the noninverting input to ground if desired.

Circuit Notation

Notation and terms used in closed loop circuits are shown in figure 9-12.2.

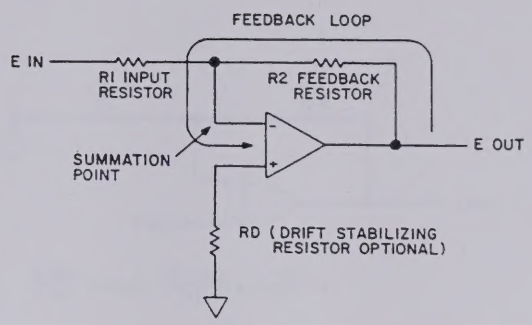


Figure 9-12.2. Circuit Notation.

The Ideal Operational Amplifier defined:

Gain - The more gain the better, since the closed-loop gain can be adjusted by resistor selection.

Input Impedance - Input impedance is assumed to be infinite. No power will be drawn by the ideal operational amplifier.

Output Impedance - Output impedance is assumed to be zero. It can supply as much current as necessary to the load being driven.

Response Time - Output occurs at the same time as input, so response time is zero. Frequency response is flat and bandwidth is infinite.

Offset - Amplifier output is zero when a zero signal appears between the input terminals. In other words, there is no offset.

Summing Point - The summing point will conduct no current to the amplifier. Also the voltage at the - and + input terminals must always be the same.

Noninverting Amplifier

Figures 9-12.1 and 9-12.2 showed the inverting amplifier configuration. Figure 9-12.3 shows the noninverting amplifier.

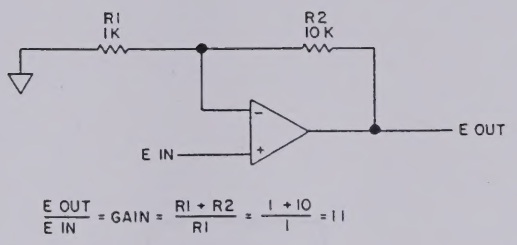


Figure 9-12.3. Noninverting Amplifier.

Voltage Follower

The circuit in figure 9-12.4 shows a variation of the noninverting amplifier where feedback is 100 percent (instead of some fraction).

Other names for this amplifier are unity gain amplifier, and source follower. The operation is explained simply by stating that no voltage difference can exist between the two-point terminals. The output must rise until it equals the input, then the amplifier is balanced. Advantages of the circuit are very high input impedance (on the order of 10 megohms) and very low output impedance (less than 1 ohm).

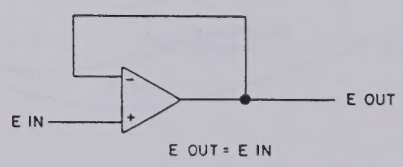


Figure 9-12.4. Voltage Follower.

Figure 9-12.5 shows a variation of figure 9-12.4. Since no current flows into or out of the operational amplifier, adding a resistance does not change the operation.

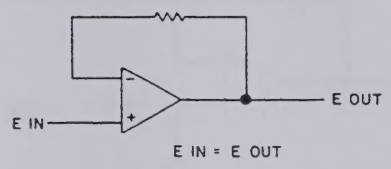


Figure 9-12.5. Voltage Follower.

Noninverting Amplifier Analysis

Figure 9-12.6 shows the noninverting amplifier circuit represented as a resistive voltage divider. The input voltage appears across R1 and the output voltage appears across the combination R1 and R2.

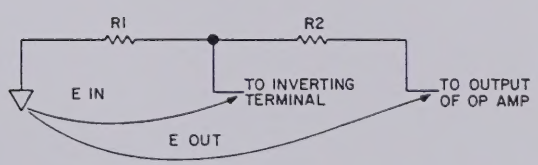


Figure 9-12.6. Resistive Divider Representing Noninverting Amplifier.

*Ein represents the voltage applied to the noninverting input which must also be applied to the inverting input. This established circuit balance.

If a capacitor is used as the feedback element in the inverting amplifier, the result is an integrator. Figure 9-12.7 shows such a circuit. Current flow through the feedback loop charges the capacitor. The capacitor remains charged until the input voltage is changed.

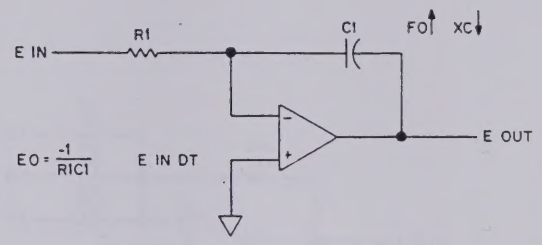


Figure 9-12.7. Integrator Circuit.

R1 x C1 Period of Signal to be Integrated

If RC time is increased, capacitor takes longer to charge. This circuit can function as a lc pass amplifier. Unity gain occurs at the frequency where Xc 1 = R1.

Voltage Adder

In a great many circuits, the input to the inverting amplifier circuit is more than one voltage Current in the feedback loop is the algebraic sum of the current due to each input. Each source, E1, E2, E3 contributes to the total current and no interaction occurs between them. All inputs "see" R1 as the input impedance, while gain is -R2/R1. Direct voltage addition may be obtained with R2 = R1. Refer to figure 9-12.8.

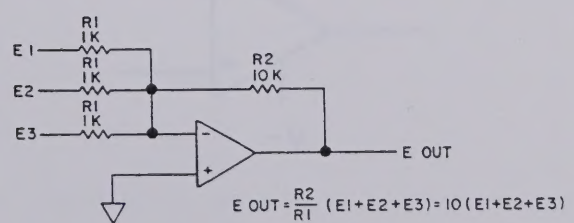


Figure 9-12.8. Voltage Adder.

Scaling Adder

A variation of the voltage adder is the scaling adder. In the scaling adder each input is "weighted" to provide the proper gain. This is shown in figure 9-12.9.

What the operational amplifier can do is limited only by the imagination and ingenuity of the user. This information sheet is only intended to scratch the surface and present some of the most commonly used circuits.

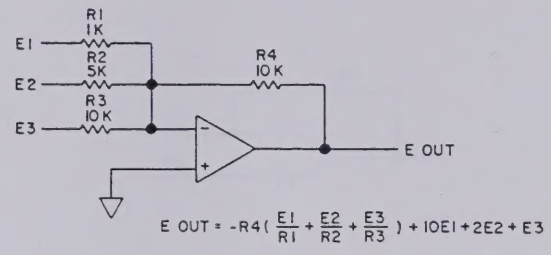


Figure 9-12.9. Scaling Adder.

If the same signal is applied to both the + and - input the two signals will be out of phase and will completely cancel each other. Since the op amp responds only to differences between its two inputs, it is said to be a differential amplifier. The voltage difference between the + input and the - input is called the differential input voltage. Since a differential amp amplifies only the differential input voltage and is unaffected by signals common to both inputs, it is said to have "common-mode" rejection. Refer to figure 9-12.10.

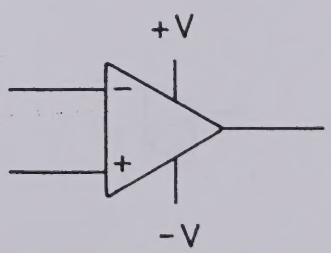


Figure 9-12.10. Differential Amplifier.

A simple way to correct for output offset due to bias currents is to use R3. Refer to figure 9-12.11.

$R3 = R111\ R2$ or $\frac{R1R2}{R1+R2}$

In some critical circuits R3 is test selected for 0 output offset voltage.

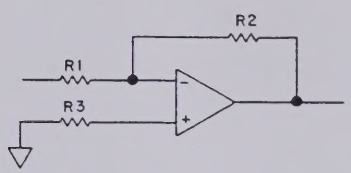


Figure 9-12.11. Differential Amplifier with Offset Correction.

Without frequency compensation (refer to figure 9-12.12) some op amp circuits will oscillate The oscillation can be stopped by compensating the op amp. This is done using a compensating cap. Frequency compensation decreases high-frequency open-loop gain. The gain of IC op amps decreases as the operating frequency increases.

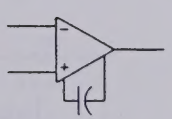


Figure 9-12.12. Differential Amplifier with Frequency Compensation.

9.13 OPERATIONAL AMPLIFIER CIRCUIT APPLICATIONS

9.13.1 Introduction

The following information is provided to aid the student in identification and troubleshooting some of the different types of operational amplifier circuits utilized in Collins equipment.

9.13.2 Circuit Applications

a. Inverting Amplifier (Refer to figure 9-13.1)

This example uses two power supplies and therefore E_{out} is capable of being driven above and below ground.

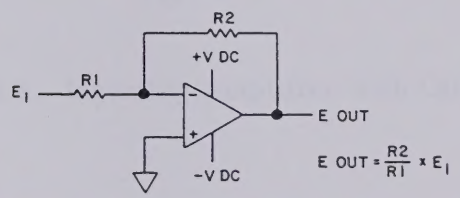


Figure 9-13.1. Inverting Amplifier.

This circuit is similar to figure 9-13.1, except the addition of R3 provides greater temperature stability. Refer to figure 9-13.2.

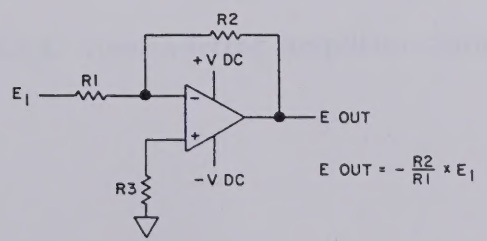


Figure 9-13.2. Inverting Amplifier with Added Temperature Stability.

This circuit operates similar to figures 9-13.1 and 9-13.2, except it has only one supply voltage. Refer to figures 9-13.3 and 9-13.4. The voltage divider R3 and R4 connected to the (+) input offsets E_{out} to a voltage level determined by the division ratio. E_{out} is now capable of being driven above and below the offset level.

b. Noninverting

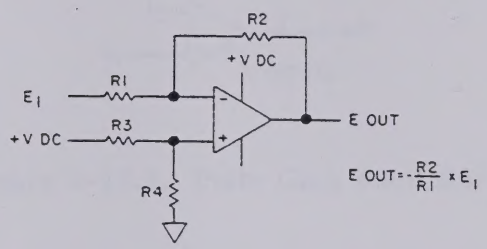


Figure 9-13.3. Inverting Amplifier with Offset Voltage.

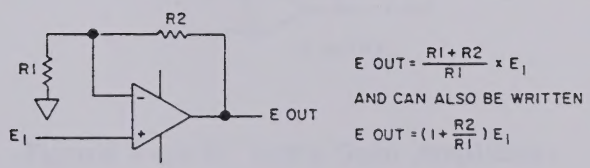


Figure 9-13.4. Noninverting Amplifier Gain Control.

c. Unit Gain (voltage follower or source follower). Refer to figures 9-13.5 and 9-13.6.

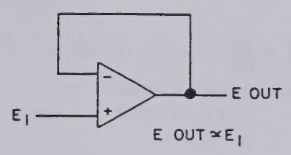


Figure 9-13.5. Unity Gain Amplifier.

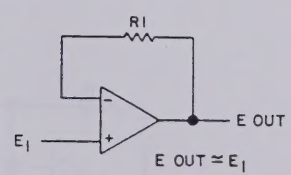


Figure 9-13.6. Unity Gain Amplifier.

d. Summing Amplifier (Noninverting) Refer to figure 9-13.7.

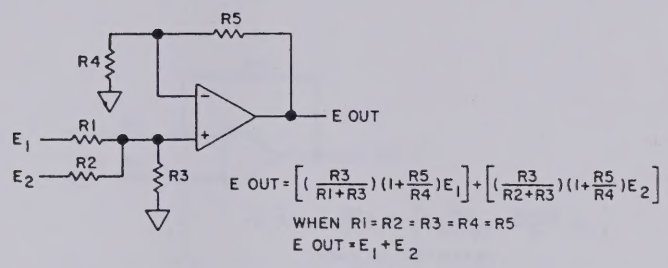


Figure 9-13.7. Noninverting Summing Amplifier.

Weighting of the inputs can be accomplished by using a different division ratio for R1 and R3 than for R2 and R3. Weighting would be necessary if the voltage at E_1 was ten times as large as E_2, but was to have the same effect on E_{out} as E_2.

e. Summing Amplifier (Inverting) Refer to figure 9-13.8.

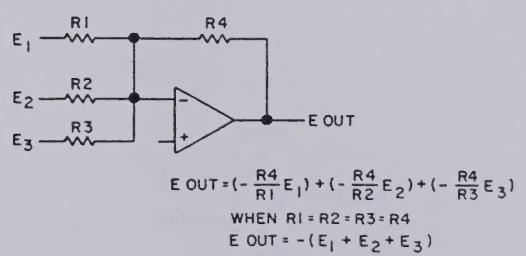


Figure 9-13.8. Inverting Summing Amplifier.

Weighting of the inputs can be accomplished by using different values of input resistors.

f. Difference Amplifier (Subtractor). Refer to figure 9-13.9.

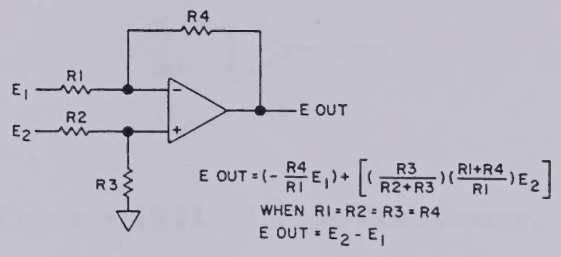


Figure 9-13.9. Difference Amplifier.

Weighting can be accomplished in the same manner as the summing amplifiers by the selection of resistor values.

g. Comparators and Voltage Detector. Refer to figures 9-13.10 and 9-13.11.

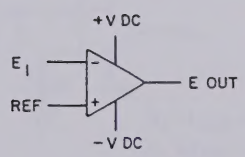


Figure 9-13.10. Voltage Comparator.

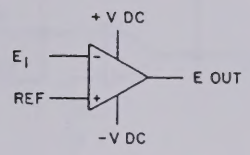


Figure 9-13.11. Voltage Comparator.

This circuit is generally operated with little or no feedback so a very slight difference between the level being monitored at E_1 and the reference will drive E_{out} to an extreme. When E_1 is less than the reference, E_{out} will be maximum positive and when E_1 is more than the reference E_{out} will be the opposite. This circuit is commonly used as a monitor with one extreme of E_{out} being an indication of good and the opposite extreme bad. It may be designed to operate from one power source or two opposite power sources whichever is required. The reference level can be established many different ways such as a voltage divider, diode, potentiometer, or by another circuit. Refer to figure 9-13.12.

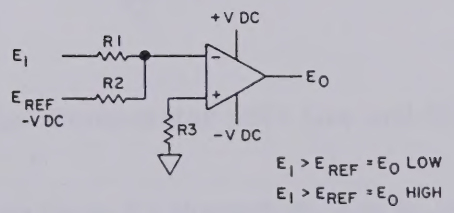


Figure 9-13.12. Voltage Comparator Using One Input.

The reference voltage can also be fed to the same input as the voltage being compared to and is generally the opposite polarity. When E_1 is more positive then E_{ref}, E_0 is held low. When E_1 is less positive than E_{ref}, E_0 is high. Since there is no limiting feedback the level of E_0 will approach the positive source voltage when high and the negative source voltage when low. By the addition of CR1 E_0 will be clamped when low to approximately 0 V dc. Refer to figure 9-13.13.

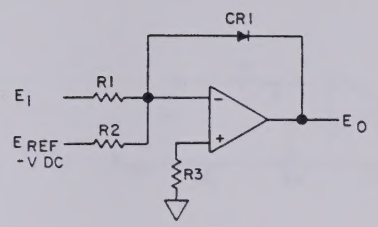


Figure 9-13.13. Voltage Comparator with Low Output Limiting.

By the addition of R_5 and R_6, E_0 when high, will be limited to a value determined by the division ratio and the positive voltage feeding it. Refer to figure 9-13.14.

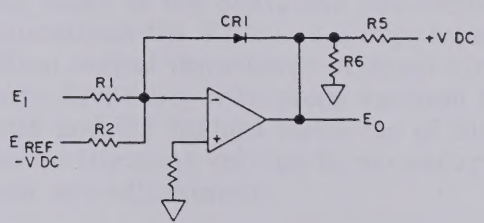


Figure 9-13.14. Voltage Comparator with Low and High Output Limiting.

By the addition of positive voltage from E_0 through R_4 and R_3 to the noninverting input E_0 can be stabilized or sensitivity can be decreased (hysteresis). When the value of E_1 becomes less than E_{ref}, E_0 switches high and applies positive voltage through R_4 and R_3 which raises the level applied to the noninverting input. E_1 must now go more positive than the new reference level to cause E_0 to switch low. R_3 can be either a variable or fixed resistor. Refer to figure 9-13.15.

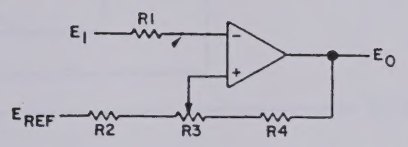


Figure 9-13.15. Voltage Comparator with Decreased Sensitivity.

9.14 FIELD EFFECT TRANSISTORS

9.14.1 Description

A field-effect transistor (FET) is a device in which the current flow is controlled by an electric field (hence, the name field-effect transistor). It works on the principle of changin current flow by changing the resistance of a channel (between source and drain) by varying the gate voltage.

In general terms the FET exhibits many of the desirable characteristics of a triode vacuum tube while still retaining many of the desirable characteristics of the conventional transistc In normal circuit configurations the FET has a high input impedance (resistance) of over 10 megohms and a medium output impedance of approximately 100,000 ohms. These impedances compare very favorably with many vacuum tube circuits, and yet the low voltag and current requirements and the instant warm-up of the ordinary transistor are still realized. Also, because no filament voltage is necessary, many of the ac hum problems that arise from this point are eliminated.

Standard terms for FET terminals have been assigned: one element is referred to as the "gate" and is abbreviated "G"; another element is referred to as the "source" and is abbreviated "S"; the final element is referred to as the "drain" and is abbreviated "D". The gate can be compared to the grid of a triode vacuum tube or to the base of a transistor the source can be compared to the cathode of a vacuum tube or to the emitter of a transistor; and the drain can be compared to the plate of a vacuum tube or to the collector of a transistor.

Figure 9-14.1 presents a simplified cross-section view of an N-channel junction FET. In theory the center portion (a resistance bar or channel), in this case N-type material, offers a predetermined resistance to the flow of current from the drain to the source (or vice-versa) electrodes. This resistance is determined by the material and the amount of impuri that is added to it. Normally this resistance will be from 100 to 2000 ohms.

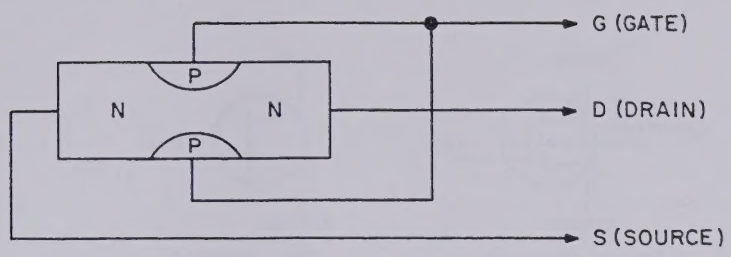


Figure 9-14.1. Cross Section View of an N-Channel Junction FET.

This resistance can be increased to almost infinity by the application of a voltage between the gate and source (or drain). In semiconductor terminology, this voltage causes a "depletion area" (an area void of current carriers -- therefore extremely high resistance) to exist around each of the P-type materials. The larger the voltage the greater the resistance, until the two depletion areas meet (this is defined as pinch-off) and the resistance increases to almost infinity.

The basic resistance bar (or channel) can be either N or P materials, hence the names N-channel or P-channel FET. The N-channel device requires a positive drain supply, and P-channel requires a negative drain supply.

There are two categories of field-effect transistors, junction field-effect transistors (JFET) and metal-oxide-silicon field-effect transistors (MOS FET -- sometimes called insulated-gate FET, or IGFET). As the names imply, a JFET uses the characteristics of a reverse-biased junction (which causes the depletion region) to control the drain-source current, while in the MOS FET the gate is a metal film deposited on an oxide layer, and is insulated from the source and drain. Both devices operate on the principle of a "channel" current controlled by an electric field. The control mechanisms for the two are different, resulting in considerably different characteristics. The main differences between the two are in the gate characteristics. The input of the JFET behaves like a reverse biased diode while the input of a MOS FET is similar to a small capacitor. The junction or the MOS may be either N or P channel, as noted in figure 9-14.1. Symbols for a junction and a MOS FET are shown in figure 9-14.2.

The field-effect transistor actually antedates the junction transistor, since Lilienfeld described it in 1928. However, due to the limited development of the physics of surface states at that time, the field-effect device of 1928 was overshadowed by the continued development of the vacuum tube. In 1948 Shockley proposed a workable field-effect device but again the FET was overshadowed, this time by the meteoric rise of the contentional transistor. Finally, in the early 1960's the FET came under persistant investigation which resulted in the junction FET and the MOS FET of today.

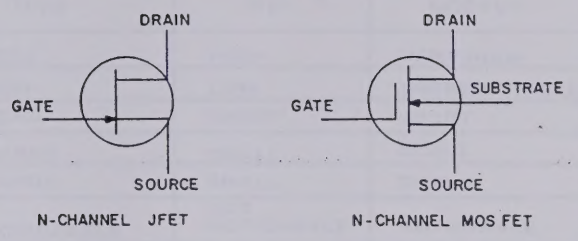


Figure 9-14.2. FJET and MOS FET Symbols.

The field-effect transistor (FET) has several advantages over the conventional transistor: it is relatively free of noise, is more resistant to the degrading effects of nuclear radiation because carrier lifetime effects are comparatively unimportant to its operation, and is inherently more resistant to burnout than a conventional (bipolar) transistor.

There are additional attributes of the FET which are advantageous for certain design considerations. The inherently high input impedance -- typically many megohms. Since it is a voltage controlled device, it can readily be "self-biased" which frequently makes for a simpler circuit than would be possible with a bipolar transistor. It also has characteristics at a drain-source voltage less than pinch-off that can be exploited for automatic gain control applications. In addition, the FET has a very high output resistance, making it useful as a constant current source when it is operated at a drain-source voltage greater than pinch-off Figure 9-14.3 illustrates a comparison of some key FET parameters and their relative magnitudes as compared to vacuum tubes and bipolar transistors. Notice that there are also significant differences between some JFET and MOS FET characteristics.

When compared with bipolar transistors, the chief short-coming of the FET is its relatively small gain-bandwidth product. This limits its use in many high-frequency applications. However, suitable FET's can provide excellent results in vhf applications, where the linearity overload resistance of the FET makes it far superior to bipolar transistors. Although the JFET is free from carrier-transmit-time limitiations, its parasitic capacitances place it at a relative disadvantage compared to MOS FET's.

From the point of view of atomic physics, the carriers in a FET do not cross a junction. Only majority carriers flow and are controlled by the electric field. Current flow in the junction transistor is by minority carriers that flow across the junction. However, we are r so much concerned about that as we are the differences in electrical characteristics and applications. The physical operations of the FET and the conventional transistor do give us the reason for some terms you have heard before -- bipolar and unipolar. A conventional transistor works because of the movement of both minority and majority carriers, hence it is called a "bipolar" device. The FET works because of a movement of majority carriers only -- therefore, it is called unipolar.

CHARACTERISTICS	VACUUM TUBE	JFET	MOS FET	BIPOLAR
INPUT IMPEDANCE	HIGH	HIGH	VERY HIGH	LOW
NOISE	LOW	LOW	UNPREDICTABLE	LOW
WARM - UP TIME	LONG	SHORT	SHORT	SHORT
SIZE	LARGE	SMALL	SMALL	SMALL
POWER CONSUMPTION	LARGE	SMALL	SMALL	SMALL
AGING	NOTICEABLE	NOT NOTICEABLE	NOTICEABLE	NOT NOTICEABLE
BIAS VOLTAGE TEMP COEFFICIENT	LOW, NOT PREDICTABLE	LOW PREDICTABLE	HIGH, NOT PREDICTABLE	LOW PREDICTABLE
TYPICAL GATE/GRID CURRENT	1 nA	0.1 nA	10 pA	–
GATE/GRID CURRENT CHANGE WITH TEMP	HIGH UNPREDICTABLE	MEDIUM PREDICTABLE	LOW UNPREDICTABLE	–
RELIABILITY	LOW	HIGH	HIGH	HIGH
SENSITIVITY TO OVERLOAD	VERY GOOD	GOOD	POOR	GOOD

Figure 9-14.3. FET Comparison Chart.

The application differences will be covered in detail later, however these are implied by the comparisons in characteristics shown in figure 9-14.3 above.

FET's are usually packaged in the same way (TO-18, plastic, TO-5, etc.) as conventional transistors.

All commercially available field-effect transistors are made of silicon and this is expected to continue.

SUMMARY

Field-effect transistors may be classified according to type of channel:

N-Channel -- made with N type silicon.
P-Channel -- made with P type silicon.

Field-effect transistors may be further classified according to method of construction:

Junction (JFET)
Insulated gate (IGFET or MOS FET)

Field-effect transistors are unipolar devices, conventional transistors are bipolar devices.

FET's are characterized by:

a. High input resistance (impedance).
b. Long operating life.
c. Extremely low power consumption.
d. Low noise.
e. Resistance to nuclear radiation.

FET's are generally inferior to conventional transistors in the areas of:

a. High-frequency switching characteristics.
b. Power handling ability.

Refer to figure 9-14.4.

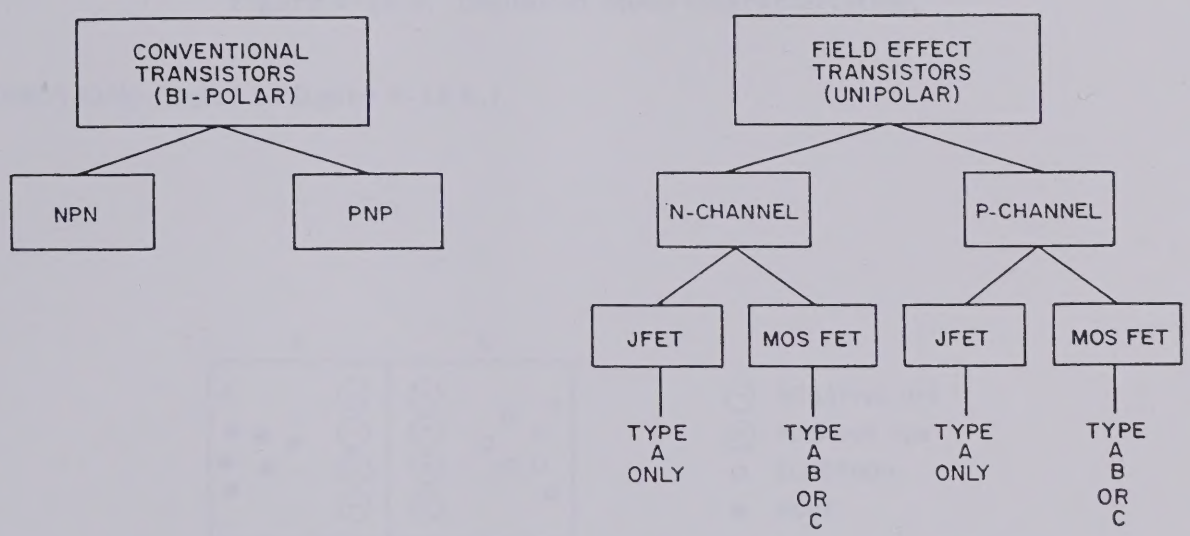


Figure 9-14.4. Classes of FETS.

CLASSES OF FETS

Type A Depletion Mode

Maximum drain current flows with no signal or voltage on the gate. Any gate voltage then "depletes" or decreases the drain current.

All JFET's are this type and MOS FET's may be this type. Refer to figure 9-14.5.

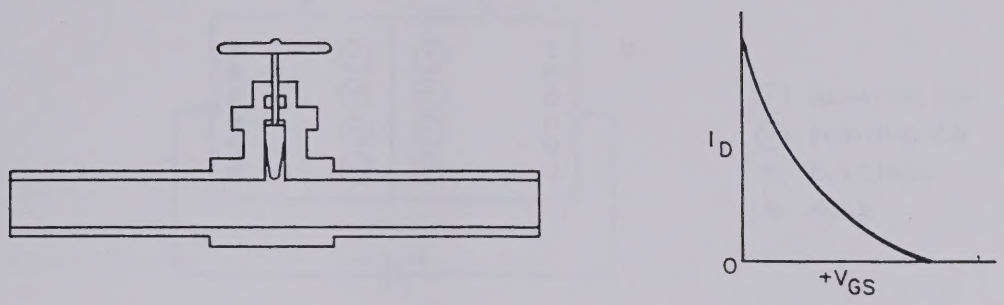


Figure 9-14.5. Depletion Mode Characteristics.

P-N JUNCTIONS (Refer to figure 9-14.6.)

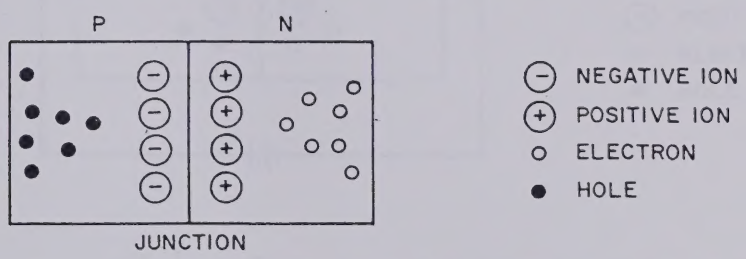


Figure 9-14.6. Formation of Potential Barrier at P-N Junction.

Refer to figure 9-14.7 for reverse biased p-n junction.

Figure 9-14.8 shows a forward-biased p-n junction. Carriers arriving at the junction cause some of the ions there to become neutral atoms, reducing the space charge.

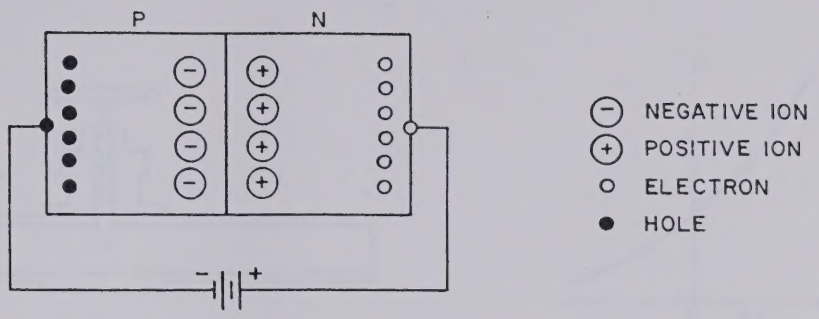


Figure 9-14.7. Reverse Biased P-N Junction.

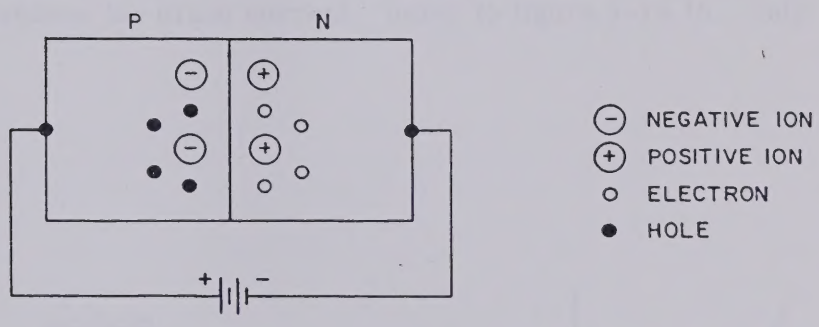
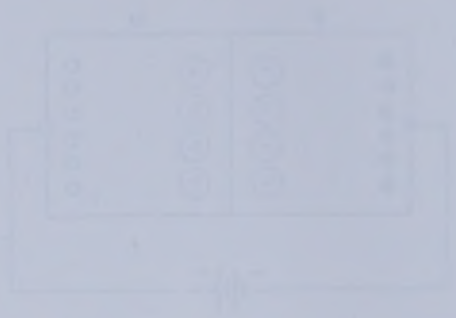


Figure 9-14.8. Forward Biased P-N Junction.

Type B Depletion -- Enhancement

Nominal drain current flows with no voltage or signal on the gate. As in the N-channel example below, a negative (-) gate voltage decreases or "depletes" drain current and a positive (+) gate voltage increases or "enhances" drain current. Refer to figure 9-14.9. Only MOS FET's are of this type.



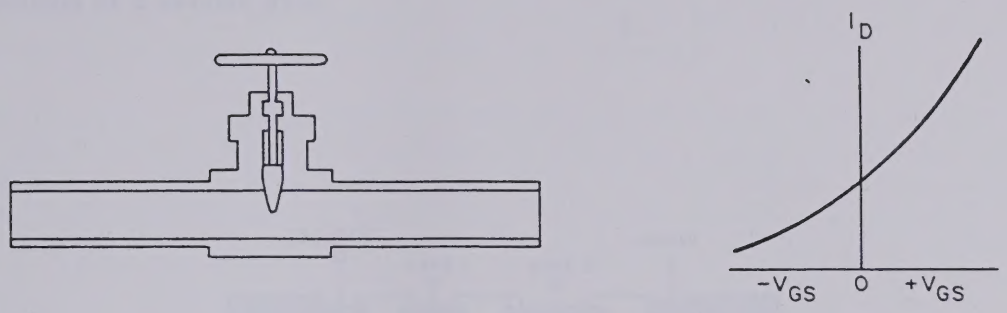


Figure 9-14.9. Depletion-Enhancement Characteristics.

Type C Enhancement Mode

Minimum drain current flows with no signal or voltage applied to the gate. Any gate voltage then "enhances" or increases the drain current. Refer to figure 9-14.10. Only MOS FET's may be this type.

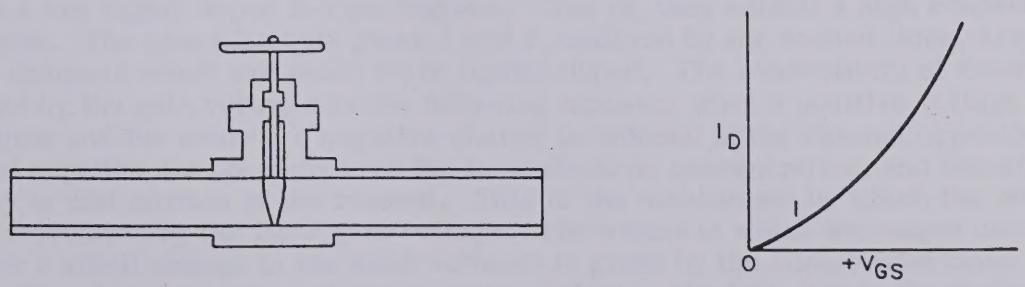


Figure 9-14.10. Enhancement Mode Characteristics.

9.15 DUAL-GATE FET OPERATION

9.15.1 Introduction

The dual-gate metal-oxide-semiconductor field-effect transistor (MOS FET) is a relatively new development in transistor technology. It has gained widespread acceptance and is currently being designed into rf amplifiers, mixers, demodulators, and other rf applications. A few reasons for its success are its high-gain, low-noise, and excellent AGC, cross-modulation, and overload characteristics.

9.15.2 Device Operation

Figure 9-15.1 shows a cross-section of the dual-gate MOSFET. The construction of the dual-gate transistor is similar to that in the single-gate MOSFET, the major difference being the addition of a second gate.

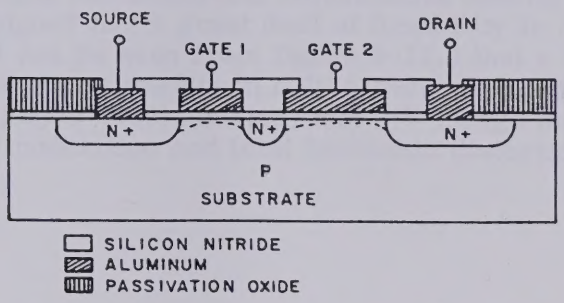


Figure 9-15.1. Dual-Gate MOS FET Cross Section.

A brief explanation of the device operation will be given for those unfamiliar with the MOSFET. Two polarities of MOSFET's are presently being manufactured, N-channel and P-channel. The channel type refers to the type of impurity used to dope the drain-to-source conduction path. For the N-type the free-charge carriers are electrons. For a P-type device, conduction is by "hole" carriers. The "N+" areas under the source and drain of figure 9-15.1 are highly doped N-type regions. That is, they exhibit a high concentration of free electrons. The areas beneath gates 1 and 2, outlined by the dashed lines, are the conduction channels which are much more lightly doped. The conductivity of these channels is controlled by the gate voltages in the following manner; when a positive voltage is applied between a gate and the source, a negative charge is induced in the channel opposite the gate. The induced negative charge increases the free-electron concentration, and therefore the conductivity in that portion of the channel. This is the mechanism by which the output current is modulated by the input gate voltage. The extent to which the output current changes (for a small change in the input voltage) is given by the transconductance (gm, yfs, ys1) and is a measure of the device's ability to amplify. Since the dual-gate MOSFET is a voltage-controlled device, once the pinch-off voltage is overcome, the output current (I_D) is dependent only on gate voltages. The pinch-off voltage is the drain-to-source voltage (V_{DS}) at which the drain current reaches a limiting value where further increases in V_{DS} do not produce any appreciable increase in the drain current.

In theory, either gate can be used for the signal input gate as both exhibit sufficient gate-to-drain transconductance. However, due to device design and certain practical considerations gate 1 functions best as the input gate. When gate 2 is used for signal injection, the channel resistance controlled by gate 1 acts as an unbypassed source resistance. Since it is impossible to bypass this degenerative source impedance, the device gain is lowered. The grounded-gate buffer and the physical separation between gate 1 and drain help achieve an extremely high degree of input-output isolation. The feedback capacitance between drain and gate 1, C_{rss}, is typically only 0.02 pF.

NOISE FIGURE

An important consideration for many low-level amplifiers is noise figure. It is often necessary in bipolar designs to sacrifice power gain to obtain the optimum noise figure. Figure 9-15.2 shows the behavior of the noise figures and power gains of a dual-gate MOSFET versus source resistance at 100 MHz and 200 MHz.

The dual-gate MOSFET offers two important advantages over most bipolar devices; very little, if any, power gain is sacrificed in achieving the best noise figure and both parameters are relatively independent of source resistance in the optimum region. These properties help alleviate the critical tuning and empirical adjustments usually required in front-end design. As a result, the designer has a great deal of flexibility in choosing a source impedance. In particular, it can be seen from figure 9-15.2 that a 3:1 change in source resistance (300 ohms to 1000 ohms) results in only a 1-dB change in noise figure. If minimum cross modulation is a prime consideration, this 3:1 change in source resistance implies a 3:1 improvement in cross modulation and total harmonic distortion for the stage.

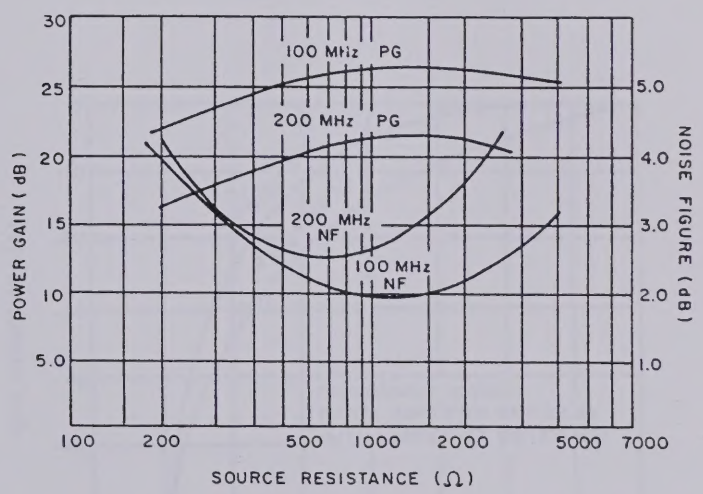


Figure 9-15.2. Dual-Gate Power Gain -- Source Resistance.

AUTOMATIC GAIN CONTROL

Most rf receivers have some means of controlling the overall receiver gain to accommodate a wide range of input signal levels. This is usually done by reducing the gain of the low-level rf and if amplifier stages. Four different methods can be used to reduce the gain of the dual-gate MOSFET: (1) forward AGC (increasing voltage) at gate 1, (2) reverse AGC at gate 1, (3) forward AGC at gate 2, and (4) reverse AGC at gate 2. Reverse AGC applied at gate 2 is superior to the other methods. Three of the AGC methods reduce gain by lowering the transconductance between gate and drain. The fourth method of gain reduction, forward AGC at gate 2, reduces the output impedance of the device.

The maximum attenuation an unneutralized rf transistor (bipolar or FET) can achieve is limited by the feedback admittance (reverse transadmittance) of the device. Due to the very low C_{rss} of the dual-gate MOSFET, gain reductions greater than 50 dB are possible at 200 MHz. Because of the increasing reactance of the feedback capacitance with decreasing frequency, 85-dB gain reduction has been achieved in a 1-MHz amplifier.

AGC APPLIED AT GATE 2

The best method of AGC is reduction of the gate-2 bias voltage from its initial optimum-gain point (greater than 4 V dc). Application of the AGC signal to gate 2 results in a remote-cutoff characteristic (remote cutoff refers to a gradual reduction in I_d with decreasing gate bias). This type of I_d-V_G characteristic contrasts with the relatively abrupt cut off of the drain current (and transconductance) when reverse AGC is applied to the gate of a single-gate MOS or junction FET. This sharp cut off produces signal clipping, increasing distortion and cross modulation. Figure 9-15.3 shows the gain reduction when the AGC signal is applied to gate 2. As the curves show, the initial gain-reduction rate is higher with a slight forward bias on gate 1 then for $V_{G1S} = 0$. This is due to the faster decrease in y_{fs} with decreasing V_{G2S} in the saturation region. This aspect of the gain-reduction rate may be useful in receiver designs where the RF AGC is delayed with respect to the if to improve overall receiver distortion.

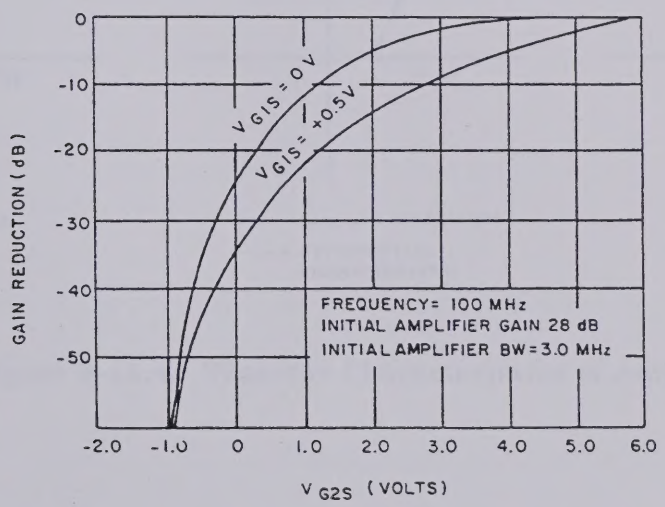


Figure 9-15.3. Gate 2 AGC Gain Reduction.

BANDWIDTH AND DETUNING

Forward AGC is usually used in bipolar amplifier designs when cross modulation and signal-handling capability are prime considerations. When this type of AGC is used, gain reduction is accompanied by a considerable increase in bandwidth and a shift in center frequency unless elaborate circuit techniques are employed. The increase in bandwidth is a result of the reduced output impedance of the bipolar device at high currents, while detuning is caused by the change in feedback and output capacitances as the output bias voltage is altered. When the AGC signal is applied to gate 2 of the dual-gate MOSFET, the output

voltage, and therefore the C_{oss}, remains constant. The output impedance does increase slightly but the output circuit is usually loaded sufficiently that its effect on the bandwidth is small. In a 200-MHz amplifier with 5-MHz bandwidth (-3 dB points), 50-dB gain reduction was accompanied by only 1.25-MHz shift in center frequency and 0.75-MHz decrease in bandwidth.

DISTORTION CHARACTERISTICS

The most attractive feature of the field-effect transistor, at least to the rf designer, is its low distortion. The square-law transfer function of the field-effect transistor results in a significant improvement in signal-handling capabilities and modulation and cross modulation distortion over that of bipolar transistors with their exponential transfer function. These transfer functions are shown in figure 9-15.4.

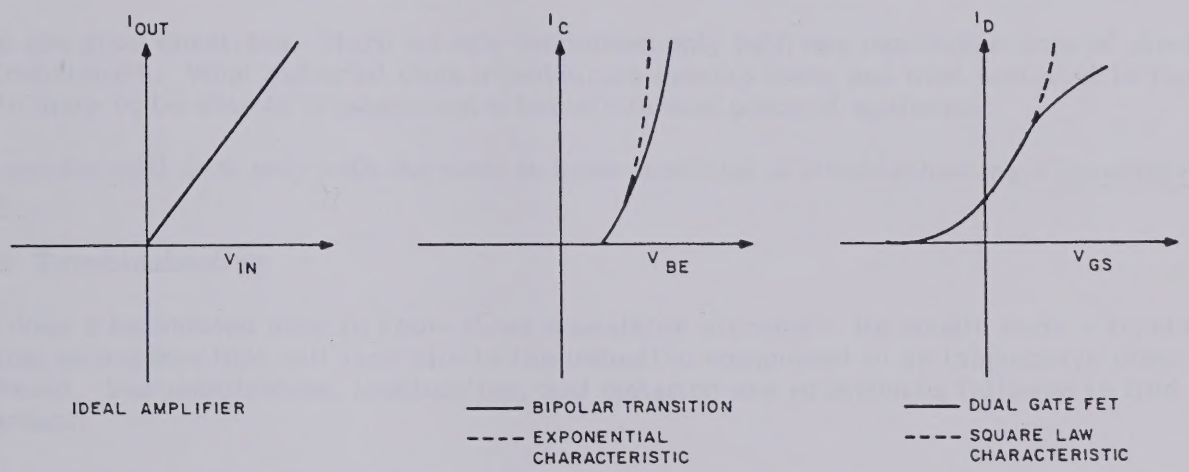


Figure 9-15.4. Transfer Characteristics of Amplifier.

MIXER OPERATION

Two basic methods of local-oscillator injection can be used with a MOSFET mixer. One uses gate 1 for both the local oscillator and signal injection. The second uses gate 1 for signal injection with the local oscillator applied to gate 2. When both the signal and local oscillator are injected at gate 1, optimum mixer performance will occur with a particular gate-1-to-source bias. The reason for this is the mechanism of the conversion process for this type of mixer operation. For an excessive local oscillator injection the device begins to saturate on the positive peaks of the local oscillator voltage. In addition to limiting the conversion gain, this clipping action also increases spurious responses.

When the local oscillator is applied to gate 2, somewhat higher injection levels are required for conversion gains comparable to the previous method. The reason for this is the lower gate-to-drain transconductance of gate 2. However, this type of injection may serve well in mixer applications where it is desirable to isolate the local oscillator from both the input and output networks.

SUMMARY

In summary, the dual-gate MOSFET should be considered for small-signal rf applications where signal-handling and distortion characteristics are important. It is especially attractive in low-level amplifiers where AGC is used.

Reference

1. "Small Signal RF Design with Dual-Gate MOSFETS." Motorola Application Note AN-478.

9.16 TRANSISTOR STAGE TROUBLESHOOTING

9.16.1 Introduction

When an electronics technician receives a defective piece of equipment, he must make this equipment operable and do it as soon as possible. How much electronic theory must this man know to effectively troubleshoot this equipment? What is the least amount of knowledge that may be presented by an instructor that will still allow this technician to do a good job?

Those are good questions. Here we are concerned only with one particular area of electronics, transistors. What material does a technician need to know and what material is just nice to know to be able to troubleshoot a transistorized piece of equipment.

This section will deal only with the need to know material of troubleshooting a transistor stage.

9.16.2 Troubleshooting

What does a technician need to know about transistor circuits? He should know a troubleshooting procedure that will lead him to the defective component in an inoperative piece of equipment. Sectionalization, localization, and isolation are procedures followed to find this component.

Sectionalization locates the trouble to a specific area in a system or piece of equipment. In a system, the trouble is sectionalized to a "black box." In a piece of equipment, such as a receiver, the trouble is located to a section, such as the power supply, oscillator or amplifier stages.

Sectionalization of a trouble in a piece of equipment does not require any special test equipment. It does require a good comprehension of the block diagram of the equipment and the ability to analyze the symptoms obtained when the equipment is inoperative.

Localization narrows down the trouble still further. It is the process of checking the inputs and outputs of each stage until a trouble area is found or measuring the voltage output of the power supply to determine its condition. Localization narrows the trouble to a defective stage or circuit.

Isolation pins down the faulty component in the stage or circuit found by localization. Voltage, resistance, and visual checks are used to isolate this component.

Sectionalization and localization of troubles in transistor circuits offer no new problems to the technician who has used these practices in vacuum tube circuits. He must know the block diagram well enough to correctly interpret any symptoms and he must trace the signal through the equipment to locate the faulty stage. He must also be able to localize the trouble

with visual, voltage, and resistance checks. However, the transistor being a solid stage device acts quite differently than a vacuum tube stage when a trouble exists. The idea of this paper is to acquaint the technician with in-circuit and out-of-circuit measurements of transistors in an inoperative stage. It will cover in-circuit voltage and resistance checks of defective stages. Out-of-circuit tests will also be made. These will include diode checks for opens and shorts, and transistor identification.

Before beginning our single stage analysis of a transistor circuit, here are some general tips on finding transistor radio troubles.

If the set is battery operated, check the battery voltage and current. The battery voltage should not change more than 10 percent from an off to on condition. (5 percent for mercury batteries.)

Look for obvious faults such as broken wires or terminals.

Worry about the transistor last. Bad transistors account for 2 to 3 percent of all transistor radio defects.

Check transistors in the circuit. The major part of this paper will be spent on how to do just that.

*Check the local oscillator with another radio. The defective radio is placed near a working radio tuned to the high end of the dial. As the defective radio is tuned through its range a whistle or squeal will be heard at some point if the defective radios oscillator is working.

Now let's begin our transistor stage checks.

*Superheterodyne receivers

IN-CIRCUIT CHECKS

Figure 9-16.1 illustrates a NPN and PNP stage and the voltage readings obtained. These readings are from each of the elements to ground. Both circuits are of the grounded negative terminal variety. The voltage readings in figure 1 and all succeeding troubleshooting examples are taken with a voltmeter of a 20,000 ohm/volt sensitivity or better.

There are a few general rules to be followed when troubleshooting any transistor stage.

RULE 1: Determine if the transistor stage is conducting. Measure the voltage across the emitter or collector resistor.

RULE 2: If a transistor stage is not conducting, check the bias to see if the transistor is being "told" to conduct.

RULE 3: The normal forward bias voltage for transistors is 0.2 volts for germanium and 0.6 volts for silicon.

TROUBLE NUMBER ONE

Now assume that resistor R4 in figure 9-16.1 opens, the voltages on the stage will appear as follows:

VOLTAGES	NPN	PNP
1. Across R_1	0 V	0 V
2. Across R_2	0 V	0 V
3. Emitter to base	0 V	0 V
4. Emitter to ground	0 V	20 V
5. Base to ground	0 V	20 V
6. Collector to ground	20 V	0 V

Refer back to our general rules. No voltage drop across R_1 or R_2 indicates that the transistor is not conducting. The emitter to base voltage is zero so the transistor is not being told to conduct. The three readings from the elements of the transistor to ground also indicate the lack of conduction. The 20 volts on the base of the PNP transistor to ground results from the low internal resistance between emitter and base. The base is assuming the emitter voltage. This sequence of voltage readings will occur when any element between the base and collector supply opens or if the base should short to ground.

TROUBLE NUMBER TWO

In figure 9-16.1, R_1 will now be the faulty component. If R_1 is open, the following voltage readings will be obtained.

VOLTAGE	NPN	PNP
1. Across R_1	5 V, plus	5 V, plus
2. Across R_2	0 V	0 V
3. Emitter to base	0 V (reverse bias)	0 V (reverse bias)
4. Emitter to ground	5 V (plus)	15 V (minus)
5. Base to ground	5 V (plus)	15 V (minus)
6. Collector to ground	20 V	0 V

The excessive voltage across R_1 can indicate a large amount of current flow or an open R_1 Other readings must be taken to determine which condition is true. The zero volts across R_2 (indicating no conduction) gives another clue to the condition of R_1. An emitter to base bias voltage of zero volts also indicates no conduction. The normal or almost normal base voltage discounts the base circuit as a source of trouble. The collector voltage is another indication of no conduction in this circuit. The emitter is assuming the base voltage and is a very definite indication of an open emitter.

TROUBLE NUMBER THREE

Assume the collector load resistor R_2 opens. The following voltages should be noted in figure 9-16.1.

VOLTAGE	NPN	PNP
1. Across R_1	Very low	Very low
2. Across R_2	20 V	20 V
3. Emitter to base	0.2 V	0.2 V
4. Emitter to ground	Very low	20 V
5. Base to ground	Low	High

A small amount of conduction is present in the emitter-base circuit as indicated by the voltage drop across R_1. The voltage across R_2 indicates no conduction here. All elements appear to have approximately the same voltage on them. Both junctions (emitter-base, base-collector) appear forward biased.

TROUBLE NUMBER FOUR

Again referring to figure 9-16.1. An internal open between emitter to base produces the following voltage readings.

VOLTAGE	NPN	PNP
1. Across R_1	0 V	0 V
2. Across R_2	0 V	0 V
3. Emitter to base	High	High
4. Emitter to ground	0 V	20 V
5. Base to ground	5 V plus	15 V minus
6. Collector to ground	20 V	0 V

The zero voltage drops across R_1 and R_2 combined with the apparently high forward bias is indicative of an internal open between emitter to base.

TROUBLE NUMBER FIVE

In figure 9-16.1, if an open develops between the base and collector leads, the following voltage readings will develop.

VOLTAGE	NPN	PNP
1. Across R_1	Low	Low
2. Across R_2	0 V	0 V

VOLTAGE	NPN	PNP
3. Emitter to base	0.2V/normal	0.2V/normal
4. Emitter to ground	Very low	20 V
5. Base to ground	Normal/low	Normal/high
6. Collector to ground	20 V	0 V

The lack of conduction, indicated by the low readings across R_1 and no voltage drop across R_2, and the normal bias voltage is a good indication of an internal open between base and collector.

TROUBLE NUMBER SIX

Refer to figure 9-16.1, the trouble is a leaky transistor. The voltages will read as follows.

VOLTAGE	NPN	PNP
1. Across R_1	High	High
2. Across R_2	High	High
3. Emitter to base	Low/reversed	Low/reversed
5. Base to ground	5 V	5 V
6. Collector to ground	Low	High

The partial short (leaky transistor) causes larger than normal voltage drops across R_1 and R_2. The combination of a large voltage across R_1 and the normal base to ground voltage may result in a reverse bias reading between the emitter and base.

High leakage is more common in small transistors. Large power transistors usually go ahead and short once they become leaky.

TROUBLE NUMBER SEVEN

In figure 9-16.1, if emitter bypass capacitor C_1 shorts, the following voltages may be expected.

VOLTAGE	NPN	PNP
1. Across R_1	0 V	20 V
2. Across R_2	High	0 V
3. Emitter to base	Normal/high	Reversed
4. Emitter to ground	0 V	0 V
5. Base to ground	0.2 V plus	Normal
6. Collector to ground	Low	0 V

The NPN transistor is conducting heavier than normal as indicated by the high voltage drop across R_2 and the low collector to ground reading. The fact that the emitter bypass of the PNP is returned to ground makes this circuit behave differently than the NPN. Shorting C_1 in the PNP circuit, reverse biases the transistor and the transistor is cut off. The zero voltage across R_2 also indicates no conduction in this circuit. The entire 20 volts is dropped across R_1.

OTHER TROUBLES

Some other transistor troubles that may occur are as follows:

1. A short between the primary and secondary of a coupling transformer will result in the primary voltage appearing at the base of the transistor connected to the secondary. The same results are true of a shorted coupling capacitor.

2. A transistor that has all normal voltages and doesn't amplify probably has an open coupling capacitor or detuned coil.

3. Shorted capacitors and the symptoms produced.

   a. If plus line electrolytics. All stage voltages are decreased, the battery current drain is increased and there may be motorboating.

   b. Electrolytic coupling capacitors. Improper base voltage to the output stage. Zero dc voltage drop across the capacitor.

   c. Bypass capacitors seldom short. They may if they're electrolytic.

REVIEW

1. A transistor is <u>not</u> conducting and has <u>no</u> forward bias voltage is not at fault. Look for trouble in the base or emitter circuit.

2. A transistor that is not conducting and has a large forward bias is probably defective.

3. A heavily conducting transistor with low or reversed bias is leaky.

4. A transistor with lower than normal conduction and normal bias has an open collector circuit. If an emitter to collector check is zero volts, the collector circuit is open. If E to C voltage is normal or slightly high, the internal collector circuit is open.

5. A transistor stage that has all <u>normal</u> dc voltages but doesn't amplify, has an open coupling capacitor or detuned coil.

IN-CIRCUIT OHMMETER CHECKS

Can resistance measurements be made effectively of a transistor that is still connected in a circuit? Yes, but it must be realized that the front-to-back ratio of the transistor will be much smaller on in-circuit checks than out-of-circuit checks.

The front-to-back ratio of a transistor junction is found by placing the ohmmeter leads across the junction, noting the resistance, reversing the leads and again noting the resistance. The two values obtained, one high and one low, indicate the front to back ratio.

A general rule can be made concerning these in-circuit resistance checks. The high resistance of the emitter-base junction and the base-collector junction should be twice the value of the low resistance.

On an in-circuit check, the low resistance for a germanium transistor should be under 500 ohms and for silicon under 1000 ohms. The high resistance reading should be twice the value of the low reading in most cases. If both readings are high, an open in the junction is indicated.

The exceptions to the two-to-one front-to-back ratios should be noted. One of these is that the emitter-base junction of the output stage in some receivers show a low reading in both directions. The other exception is that power transistors in output stages will show a low resistance because of the shunting effect of circuit resistances. Once these exceptions are noted there should be little confusion.

There are few "zero ohm" shorts when a transistor fails. The exception is when a power transistor fails. How can a transistor be checked for partial shorts? The best method is to read the voltages and understand what produces them.

OUT-OF-CIRCUIT TESTS

Figure 9-16.2 illustrates the dc equivalent circuit of a PNP transistor. This is how the circuit would appear to an ohmmeter. Between the base and emitter and base and collector are diodes. Between the emitter and collector is a diode in series with a fairly large resistance. With an ohmmeter connected across the emitter to base diode or base collector diode observe the reading. Reverse the meter leads and again observe the reading. One reading should be high and one should be low indicating a good front-to-back ratio. In some small transistors the high reading may appear as an open. The transistor is not open if the low reading can be obtained. If the low reading cannot be obtained in one direction of the ohmmeter leads, then it is safe to assume that one of the transistor leads is open. The following table shows some transistor types and the readings to expect.

TYPE OF STAGE	OHMMETER RANGE	FORWARD	REVERSE
Rf, If, Audio Driver (Silicon)	RX100	100 ohms or less	Very high
Rf, If, Audio Driver (Germanium)	RX100	500 ohms or less	Very high
Large Power Units	RX10 or RX100	100 ohms or less	Over 5000

LEAKAGE CHECKS

When making an emitter to collector leakage test, be sure to use the proper range. RX100 or RX1000 for low power rf and if types. RX10 ro RX100 for audio drivers. RX1 for large power transistors. The front-to-back ratio is of no concern here. Our previous diode checks have established the most important of these ratios. What are we looking for?

When the resistance between the emitter and collector is zero or when it changes or drifts quickly after the ohmmeter is connected, the transistor is defective.

IDENTIFYING TRANSISTOR TYPES

The transistor type (NPN or PNP) can be identified when the polarity of the ohmmeter battery is known. Repeat the diode checks as shown previously. When a low resistance reading is obtained across a transistor junction, the polarity of the ohmmeter matches the interval polarity of the transistor. The Negative voltage is on the N material and the Positive voltage on the P material. NOTE! The emitter and collector are always of the same type material. The base is always of the opposite type.

GAIN CHECKS

Gain checks are sometimes put forth as a transistor check. This check, which is a dc check, has almost nothing to do with the way a transistor will perform in a practical rf circuit. Too many other factors such as input and output impedance, or biasing, are involved. The best gain check is an in-circuit check measuring the ac input and output of the stage.

REVIEW

1. In most cases, an in-circuit resistance reading of a transistor should show the high resistance of a junction (emitter-base, base-collector) to be twice the low resistance of that junction.

2. If both resistance readings of a transistor junction are high, an open is indicated.

3. Few transistor shorts are of the "zero ohm" variety. The exception is the power transistor short.

4. The proper ohmmeter range must be used when making an emitter to collector leakage test. A zero reading or changing reading indicates a defective transistor.

5. The transistor type can be identified if the polarity of the ohmmeter battery is known.

SUMMARY

A simple and practical approach to translator troubleshooting has been presented. It is hoped that this information sheet will help the technician to quickly find the majority of transistor troubles. Not all possibilities were presented here. Those that were presented were to show the unique conditions that develop in a defective stage.

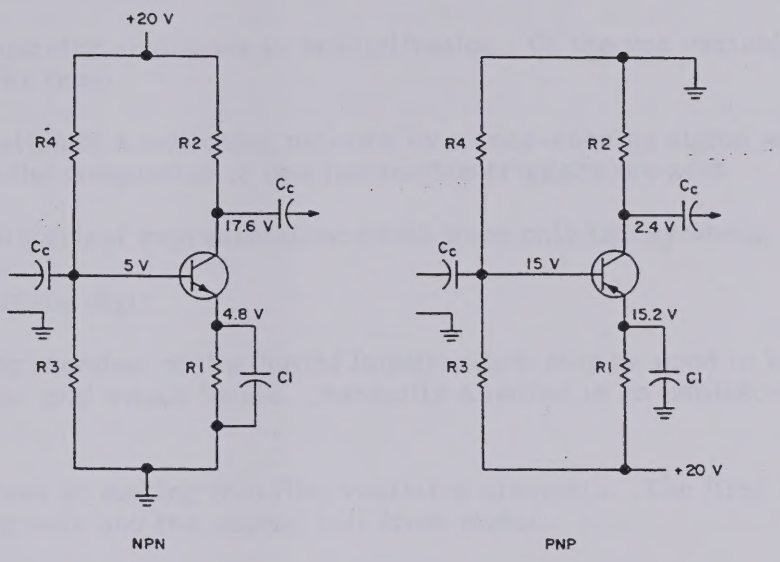


Figure 9-16.1. NPN and PNP Transistor Circuits.

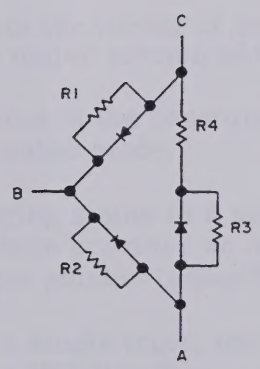


Figure 9-16.2. DC Equivalent of Transistor Circuit.

9.17 COMPUTER AND INTEGRATED-CIRCUIT GLOSSARY

ACTIVE ELEMENTS--Those components in a circuit which have gain or which direct current flow: diodes, transistors.

ADDER--Switching circuits which generate sum and carry bits.

AND--A Boolean logic operator analogous to multiplication. Of the two variables, both must be true for the output to be true.

ASYNCHRONOUS--Operation of a switching network by a free-running signal which triggers successive instructions; the completion of one instruction triggers the next.

BINARY--A system of numerical representation which uses only two symbols, 0 and 1.

BIT--Abbreviation for binary digit.

BUFFER--A noninverting member of the digital family which may be used to handle a large fan-out or to convert input and output levels. Normally a buffer is an emitter-follower type of circuit.

CERMET--A material used in making thin film resistive elements. The first half of the term is derived from ceramic and the second half from metal.

CHIP--A single substrate on which all the active and passive elements of an electronic circuit have been fabricated utilizing the semiconductor technologies of diffusion, passivation, masking, photoresist, and epitaxial growth. A chip is not ready for use until it is packaged and provided with terminals for connection to the outside world. Also called a dip.

CLEAR--To restore a memory or storage device to a "standard" state, usually the "zero" state.

CLOCK--A pulse generator which controls the timing of switching circuits and memory states, and equals the speed at which the major portion of the computer operates.

CML: CURRENT-MODE-LOGIC--Operates in the unsaturated mode as distinguished from all other forms which operate in the saturated mode.

COUNTER--(a) A device capable of changing states in a specified sequence upon receiving appropriate input signals; (b) a circuit which provides an output pulse or other indication after receiving a specified number of input pulses. (Specific counters follow.)

COUNTER, BINARY--A flip-flop having a single input, each time a pulse appears at the input, the flip-flop changes state; called a "T" flip-flop.

COUNTER, RING--A loop or circuit of interconnected flip-flops so arranged that only one is "on" at any given time and that as input signals are received, the position of the "on" state moves in sequence from one flip-flop to another around the loop.

DCTL: DIRECT-COUPLED TRANSISTOR LOGIC--Logic is performed by transistors.

DECIMAL--A system of numerical representation which uses ten symbols, 0, 1, 2, 3, ... 9.

DELAY--Undesirable delay effects are caused by rise time and fall time which reduces circuit speed, but intentional delay units may be used to prevent inputs from changing whil clock pulses are present. The delay time is always less than the clock pulse interval.

DIFFUSION--A thermal process which introduces tiny amounts of impurities into the base material. A difficult process in solids though quite easy in fluids. Just drop a bit of colo ing matter in a glass or water and the color will very gradually distribute itself throughou the water.

DIGITAL CIRCUIT--A circuit which operates like a switch, that is, it is either "on" or "of

DISCRETE--Electronic circuits built of separate, finished components.

DTL: DIODE-TRANSISTOR-LOGIC--Logic is performed by diodes. The transistor acts a an amplifier; and the output is inverted.

EPITAXIAL GROWTH--A chemical reaction in which silicon is precipitated from a gaseou solution and grows upon the surface of a silicon water present in the gaseous solution.

EXCLUSIVE "OR"--The output is true if either of two variables is true, but not if both are true.

FALL TIME--A measure of the time required for a circuit to change its output from a high level(1) to a low level(0).

FAN-IN--The number of inputs available on a gate.

FAN-OUT--The number of gates that a given gate can drive. The term is applicable only within a given logic family.

FEB--Acronym for functional electronic block. Another name for a monolithic integrated circuit.

FLIP-FLOP--An electronic circuit having two stable states, and having the ability to chang from one state to the other upon the application of a signal in a specific types below.

FLIP-FLOP "D"--D stands for delay. A flip-flop whose output is a function of the input which appeared one pulse earlier, that is, if a 1 appears at its input, the output a pulse later will be a 1.

FLIP-FLOP "J-K"--A flip-flop having two inputs designed J and K. At the application of a clock pulse, a 1 on the J input will set the flip-flop to the 1 or "on" state; a 1 on the K input will reset it to the 0 or "off" state, and 1's simultaneously on both inputs will cause it to change state regardless of what state it had been in.

FLIP-FLOP "R-S"--A flip-flop having two inputs designed R and S. At the application of a clock pulse, a 1 on the S input will set the flip-flop to the 1 or "on" state, and 1 on the R inp will reset it to the 0 or "off" state. It is assumed that 1's will never appear simultaneously at both inputs.

FLIP-FLOP "R-S-T"--A flip-flop having three inputs, R, S, and T. The R and S inputs produce states as described for the R-S flip-flop above; the T causes the flip-flop to change states.

FLIP-FLOP "T"--A flip-flop having only one input. A pulse appearing on the input will cause the flip-flop to change states.

GATE--A circuit having two or more inputs and one output, the output depending upon the combination of logic signal at the inputs. There are four gates called: AND, OR, NAND, NOR. The definitions below assume positive logic is used.

GATE, AND--All inputs must have 1-state signals to produce a 1-state output.

GATE, NAND--All inputs must have 1-state signals to produce an 0-state output.

GATE, NOR--Any one input or more having a 1-state signal will yield an 0-state output.

GATE, OR--Any one input or more having a 1-state signal is sufficient to produce a 1-state output.

GIGO--An acronym used to describe a computer whose operation is suspect. (Garbage in, garbage out.)

HALF-SHIFT REGISTER--Another name for flip-flop.

HYBRID--A method of manufacturing integrated circuits by using a combination of the monolithic and thin film methods.

INTEGRATED CIRCUIT--The Electronic Industries Association defines the semiconductor integrated circuit as--"the physical realization of a number of electrical elements inseparably associated on or within a continuous body of semiconductor material to perform the functions of a circuit."

INVERTER--The output is always in the opposite logic state of the input. Also called a NOT circuit.

LINEAR CIRCUIT--A circuit whose output is an amplified version of its input, or, whose output is a predetermined variation of its input.

MONOBRID--A method of manufacturing integrated circuits by using more than one monolithic chip within the same package.

"NOT"--A Boolean logic operator indicating negation. A variable designated "not" will be the opposite of its "and" and "or" function. A switching function for only one variable.

"OR"--A Boolean operator analogous to addition. (Except that two truths will only add up to one truth.) Of two variables, only one need be true for the output to be true.

PARALLEL OPERATION--Pertaining to the manipulation of information within computer circuitry in which the digits of a word are transmitted simultaneously on separate lines. Faster than serial operation, but requires more equipment.

PASSIVE ELEMENTS--Those components in a circuit which have no gain characteristics, capacitors, resistors, or inductors.

POSITIVE LOGIC--The more positive voltage (or current level) represents the 1-state to propagate through a chain of circuit elements.

RCTL: RESISTOR-CAPACITOR-TRANSISTOR-LOGIC--Same as RTL except that capacitors are used to enhance switching speed.

REGISTER--A device used to store a certain number of digits within the computer circuitry, often one word. Certain registers may also include provisions for shifting, circulating, or other operations.

RTL: RESISTOR-TRANSISTOR-LOGIC--Logic is performed by resistors. The transistor produces an inverted output from any positive input.

SERIAL OPERATION--Pertaining to the manipulation of information within computer circuitry, in which the digits of a word are transmitted one at a time along a single line. Though slower than parallel operation its circuitry is considerably less complex.

SKEWING--Refers to time delay or offset between any two signals.

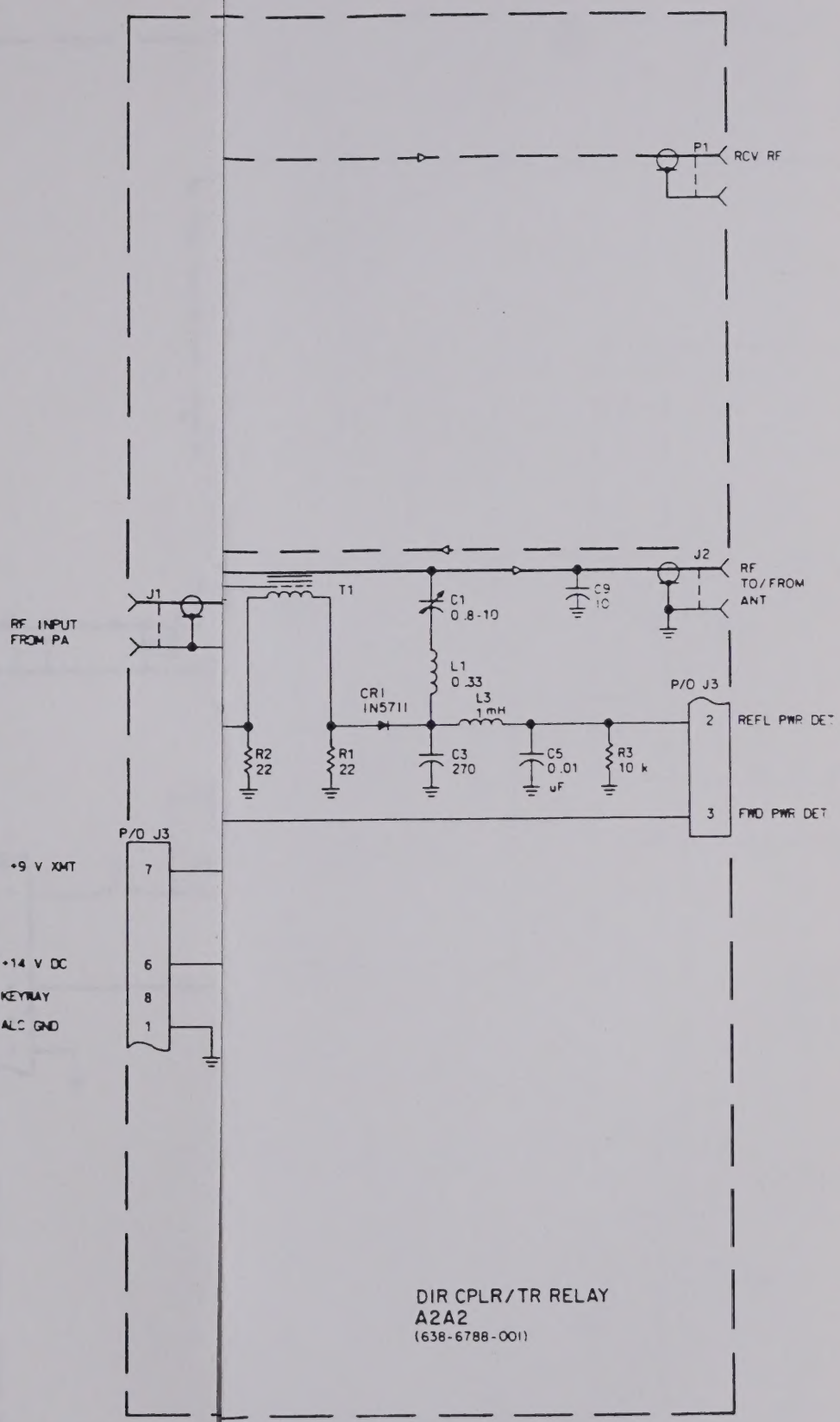
SKEWING RATE--Refers to rate at which output can be driven from limit to limit over the dynamic range.

SYNCHRONOUS--Operation of a switching network by a clock pulse generator. Slower and more critical than asynchronous timing but requires less and simpler circuitry.

THIN FILM--A method of manufacturing integrated circuits by depositing thin layers of materials to perform electrical functions; usually only passive elements are made this way.

TTL: TRANSISTOR-TRANSISTOR-LOGIC--A modification of DTL which replaces the diode cluster with a multiple-emitter transistor.

WORD--The term "word" denotes an assemblage of bits considered as an entity in a computer.



ow-Pass Filter Diagram.

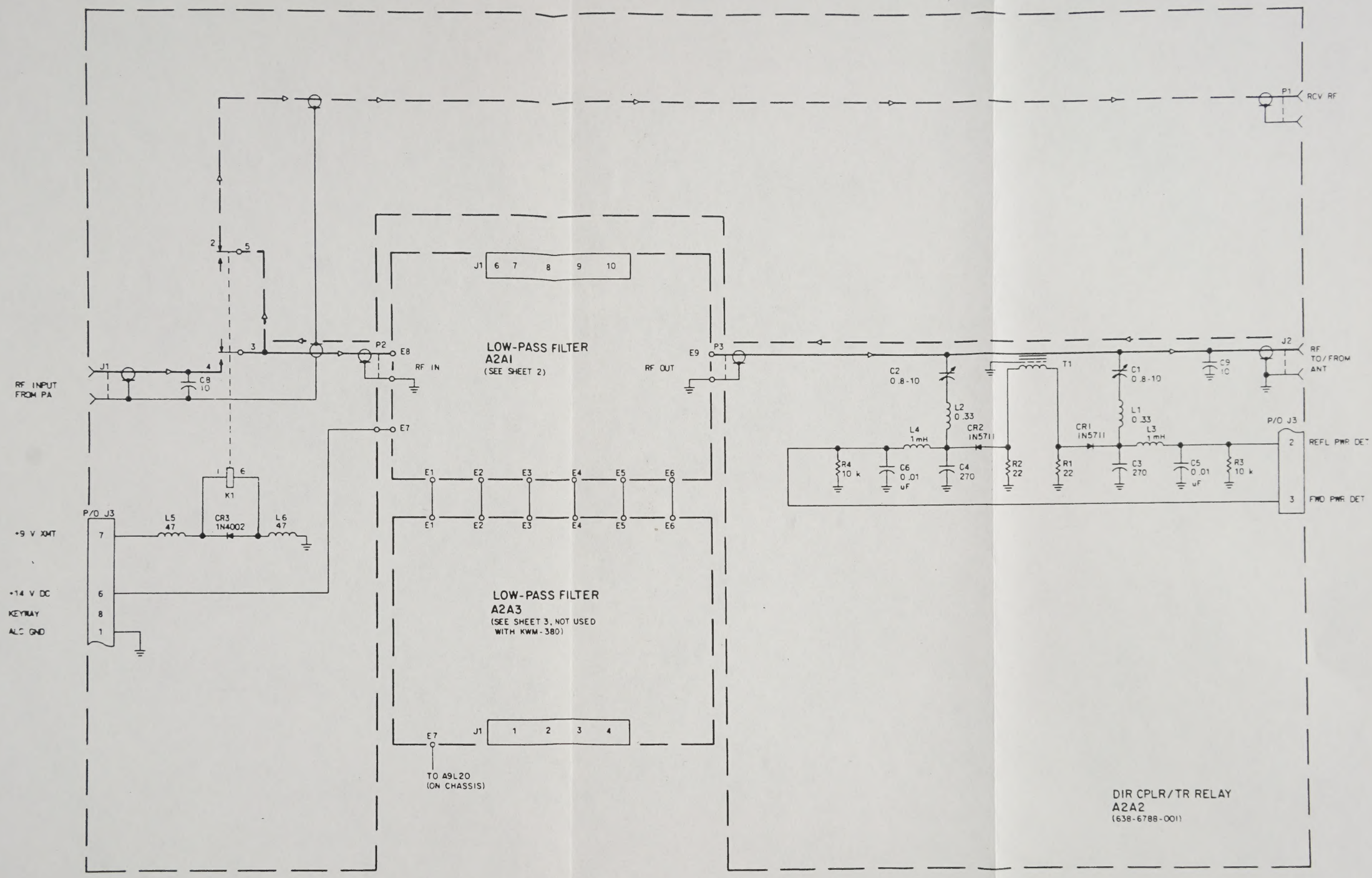
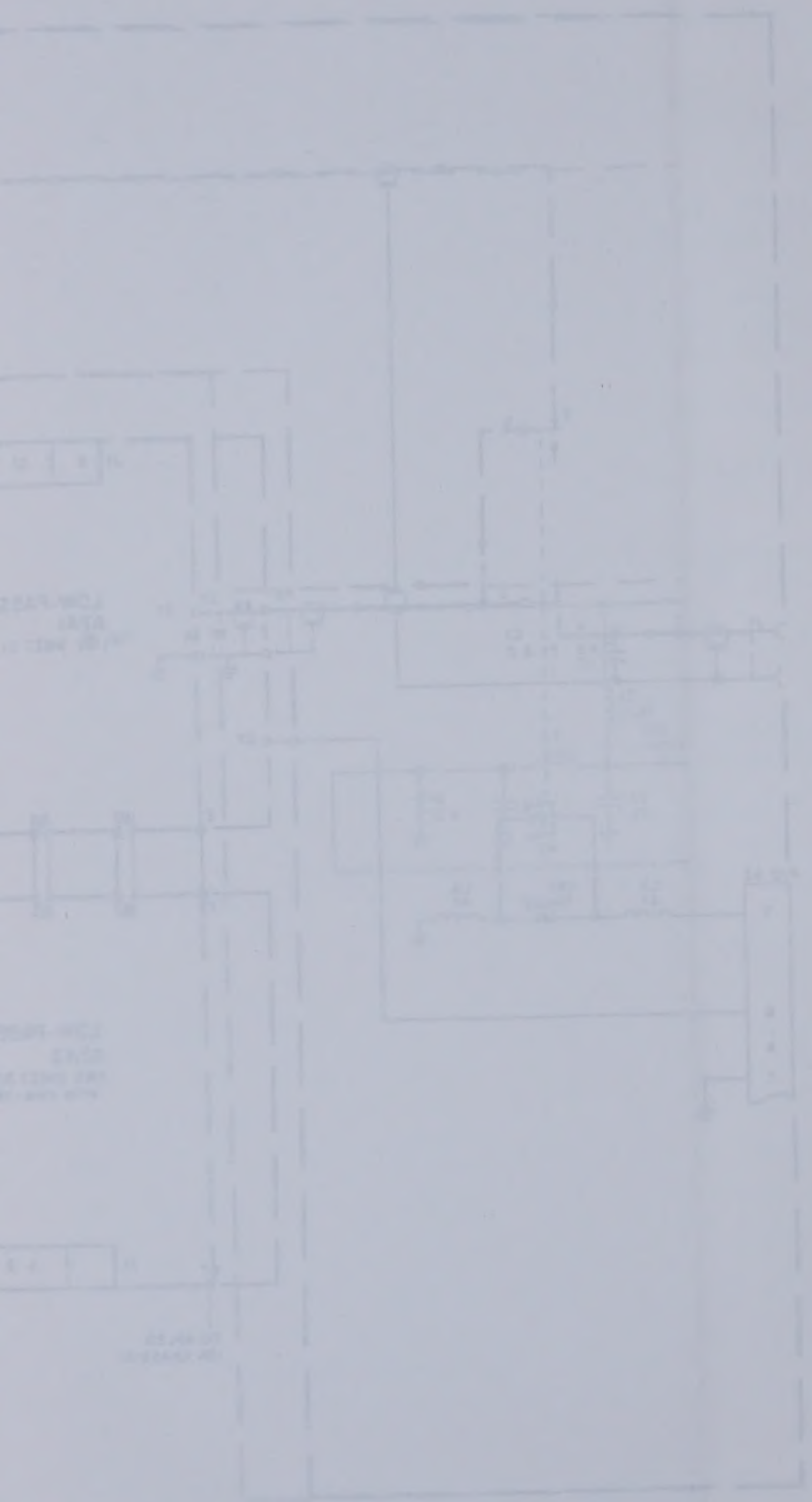
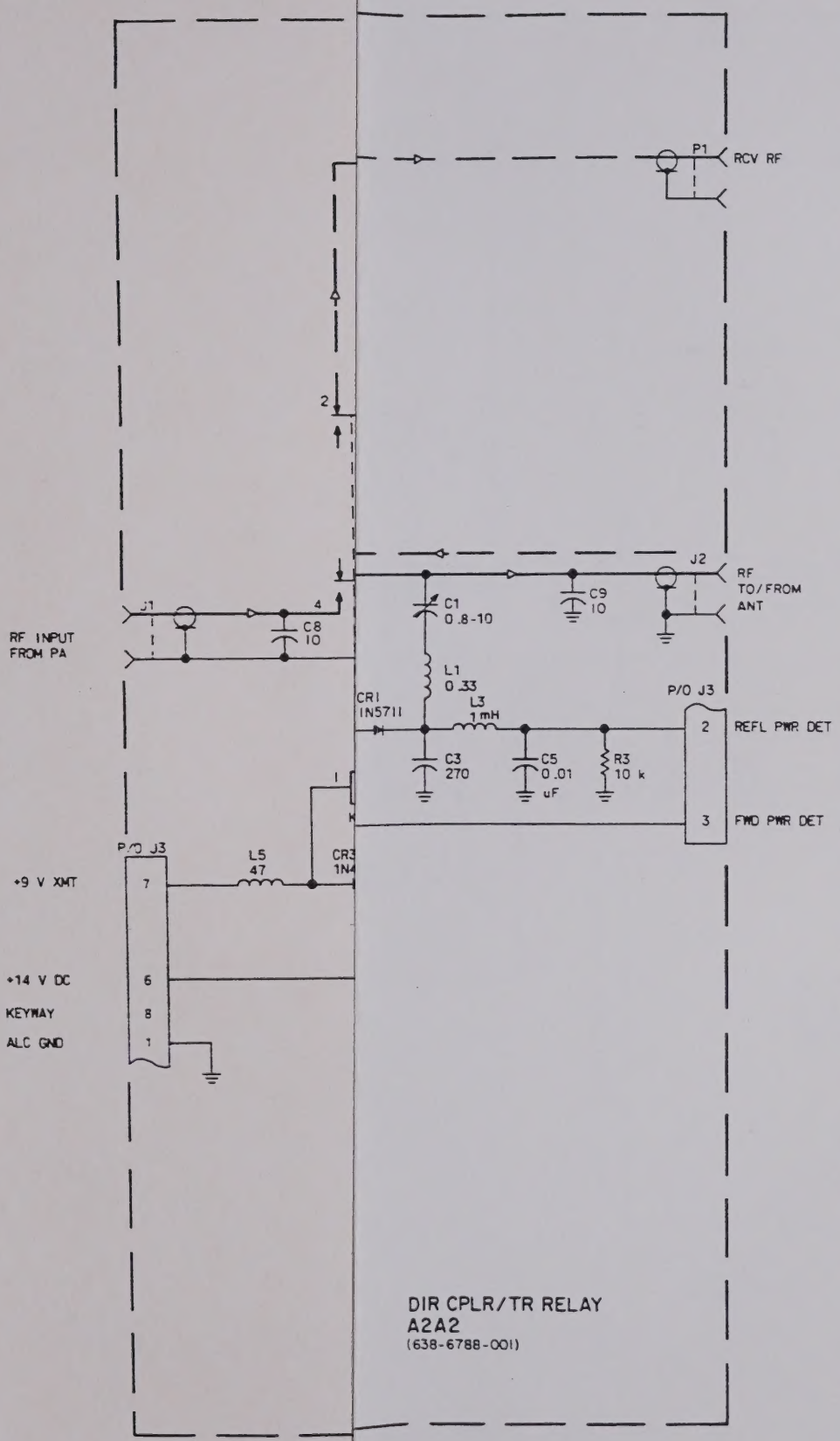


Figure 4-11. Low-Pass Filter Diagram.





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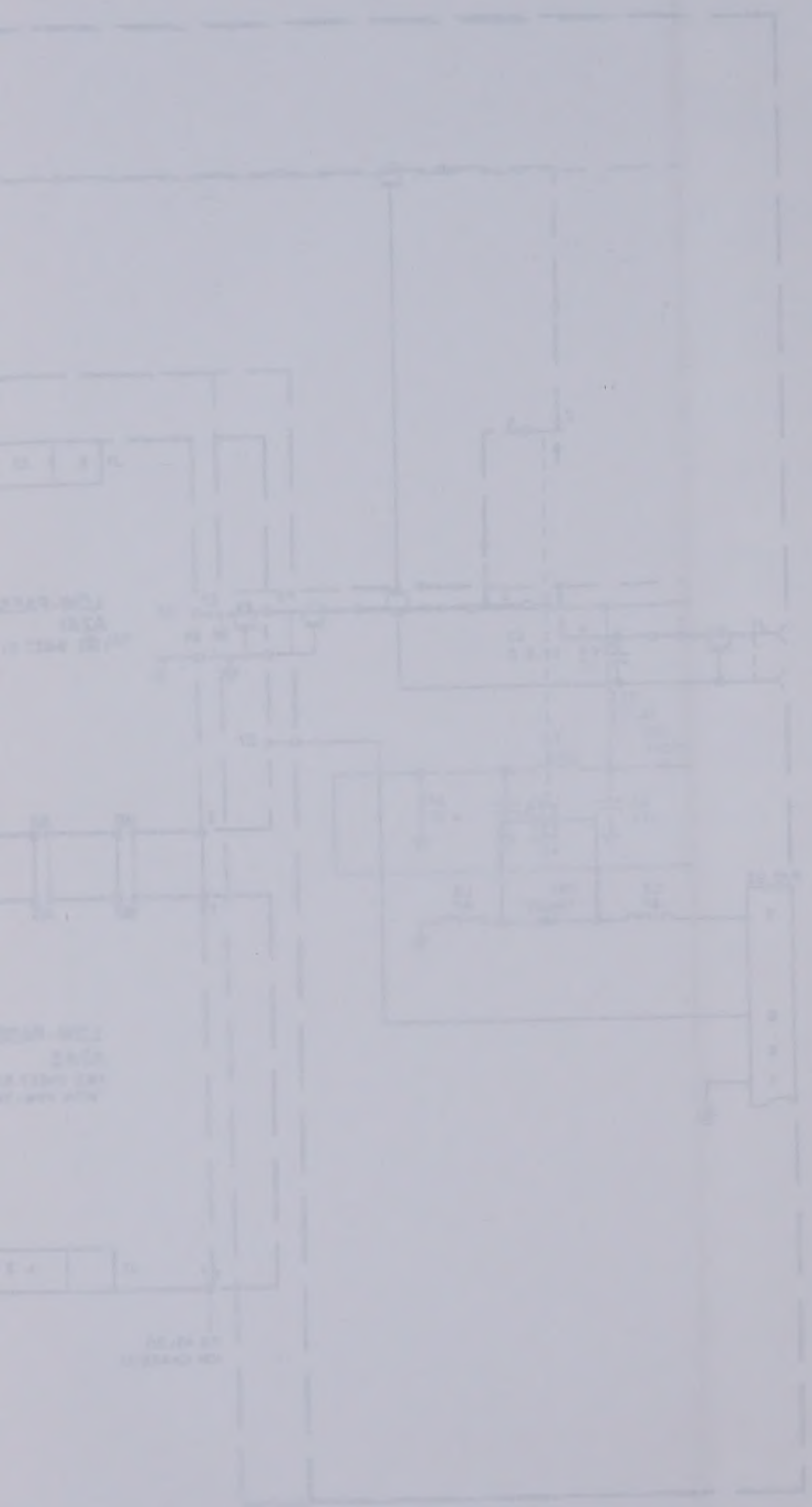
-Pass Filter Assembly A2.



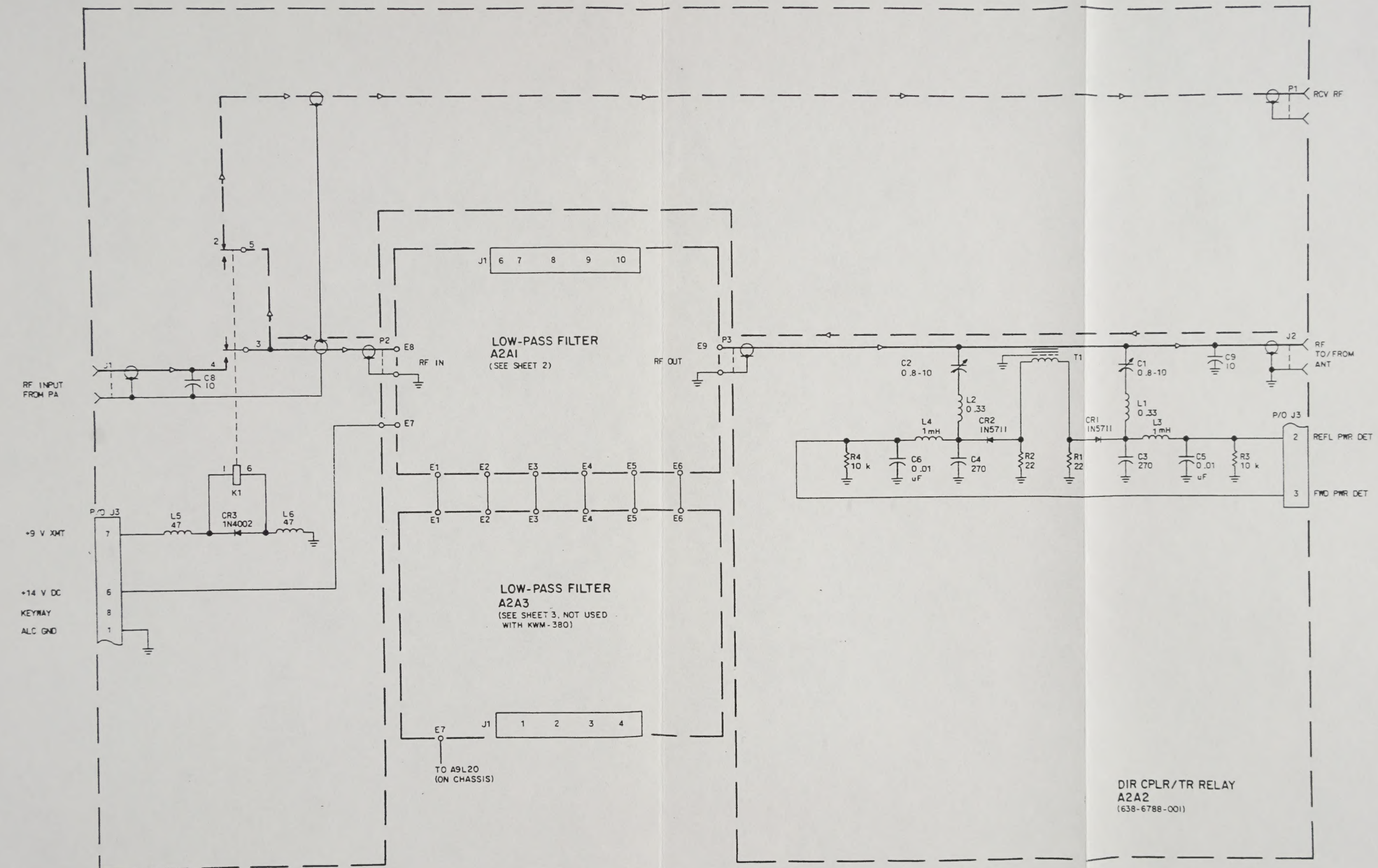


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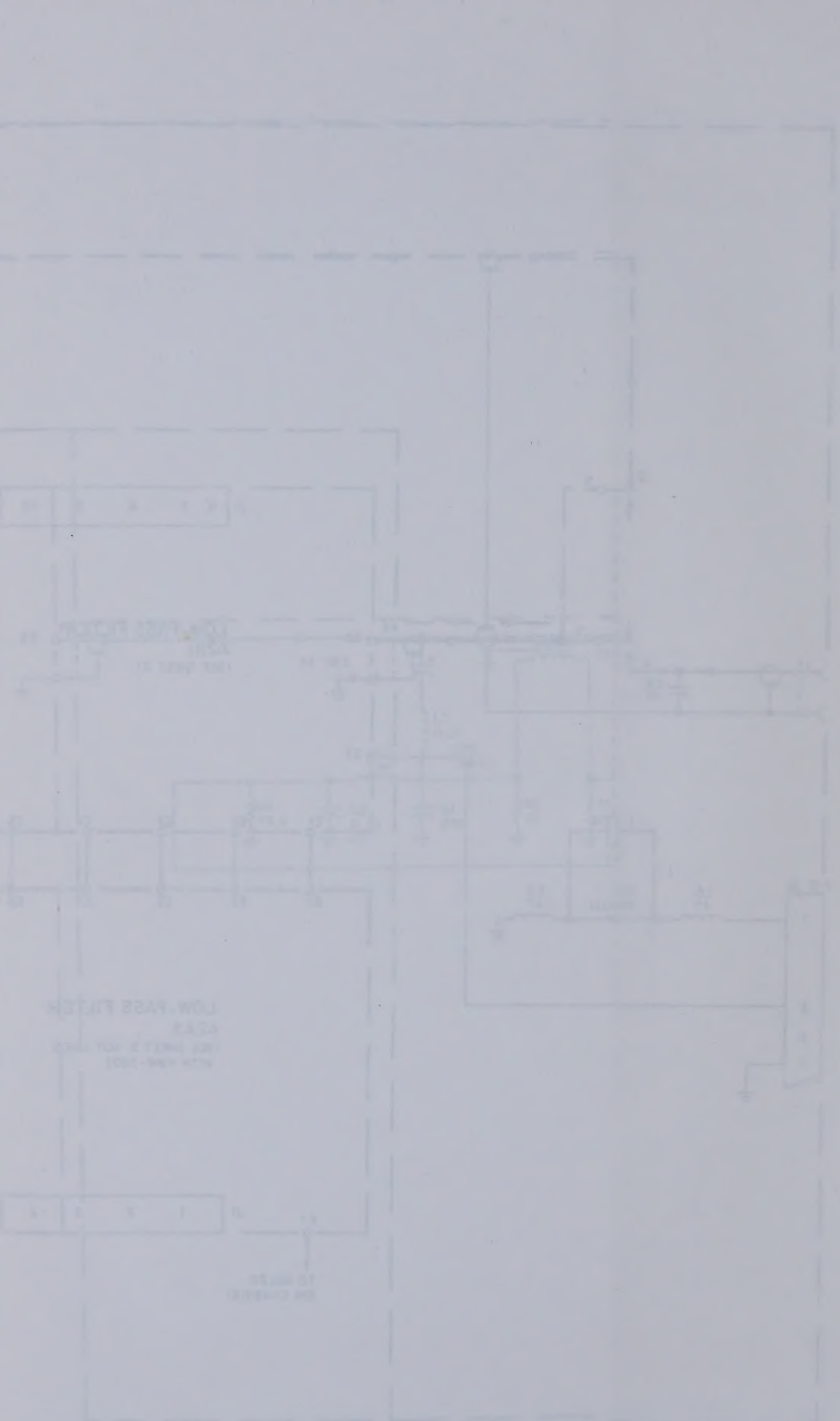
Figure 3-2. Low-Pass Filter Assembly A2.



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